DC Stability of Nullator-Norator-Modeled Resistive Networks Realized with Transistors

Yoshinobu KATO and Tadashi MATSUMOTO

Abstract —— A DC stability criterion for the transistorized nullator-norator-modeled resistive networks is proposed. DC stability essentially depends on the selection of pairs of nullators and norators, and it can be checked by using the return difference matrix. A nullator-norator circuit corresponding to Schmitt trigger is illustrated as an example. The experimental results using transistors are also shown.

1. Introduction

In 1960, Oono [1] introduced the singular network elements into the active network theory, and pointed out that they correspond to the ideal transistors, for which the base currents are zero and the base-emitter voltages are zero (or equivalently, $h_{ie}=0$ and $h_{fe}=\infty$). Afterward, the singular network elements were named "nullators" and "norators" [2], and the nullator-norator pair was termed "the nullor" [3].

Today, the nullator-norator concept is widely used in the area of electronic circuit, active network theory and graph theory. The reasons for this are as follows: (1) There exist practical electronic devices of nullors, such as transistors, FET's and operational amplifiers. (2) By applying the nullator-norator equivalent transformations to a known electronic circuit, some new electronic circuits may be derived [4]. (3) The analysis and synthesis of electronic circuit by using nullators and norators are relatively simple [5]-[7].

In the realization of nullator-norator-modeled networks with practical electronic devices, the stability problem and the bias problem must be investigated [7]-[13]. The stability problem includes the selection of pairs of nullators and norators, and the determination of input- and output-polarities of practical electronic devices. The bias problem, if transistors are used, includes the selection of types of transistors (npn or pnp), and the determination of the connection of resistors to positive- or negative-DC voltage supplies or ground. The stability problem for operational amplifiers has been discussed in many literatures [7]-[9], [12], but it for transistors or FET's has not been discussed except for literatures [10], [11], [13].

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This paper describes the stability problem in realizing nullator-norator-modeled resistive networks with transistors [11]. Stability of the realized transistor circuits is analyzed by using the return difference matrix [14] for the associated controlled-source-modeled resistive networks. A nullator-norator circuit corresponding to Schmitt trigger [15] is illustrated as an example. The experimental results of realized transistor circuits are shown. They agree with the stability analysis which is based on the return difference matrix.

2. DC Stability of Transistorized Nullator-Norator-Modeled Resistive Network

2.1 Formulation of Nullator-Norator-Modeled Resistive Network N

[Definition 1] A nullator-norator-modeled resistive notwork N consists of independent-voltage-sources e_1 (their currents : i_1), independent-current-sources j_0 (their voltages : v_0), m nullators (their voltages : $v_5 \equiv 0$, their currents : $i_5 \equiv 0$), m norators (their voltages : v_6 = arbitrary, their currents : i_6 = arbitrary), and positive-valued resistors. And the network N has a unique solution.

From this definition, the following Lemma holds.

[Lemma 1] The network N has no tie-set consisting of independent-voltage-sources and/or nullators (norators), and no cut-set consisting of independent-current-sources and/or nullators (norators).

2.2 Formulation of Controlled-Source-Modeled Resistive Network $\mathcal{N}$

In realizing the nullator-norator-modeled resistive network N with transistors, (1) all nullator-norator pairs must be chosen in three-terminal configuration, and (2) the positive direction of the polarity of transistor in respect to the signal, must be chosen so that the base current and the collector current flow into the transistor, without distinction of type of transistor (npn or pnp). For the stability analysis of the realization circuit using transistors, CCCS's (Current-Controlled Current-Sources) are used as macro-models of transistors. Fig. 1 shows the relation among nullor (i.e., nullator-norator pair), transistor and CCCS.

[Definition 2] A controlled-source-modeled resistive network $\mathcal{N}$ is the network that nullators are replaced by current-sensors e_2 (their currents : i_2), and norators are replaced by controlled-current-sources i_8 (their voltages : v_8) in the network N.

The network $\mathcal{N}$ is written by the following hybrid equation [14]

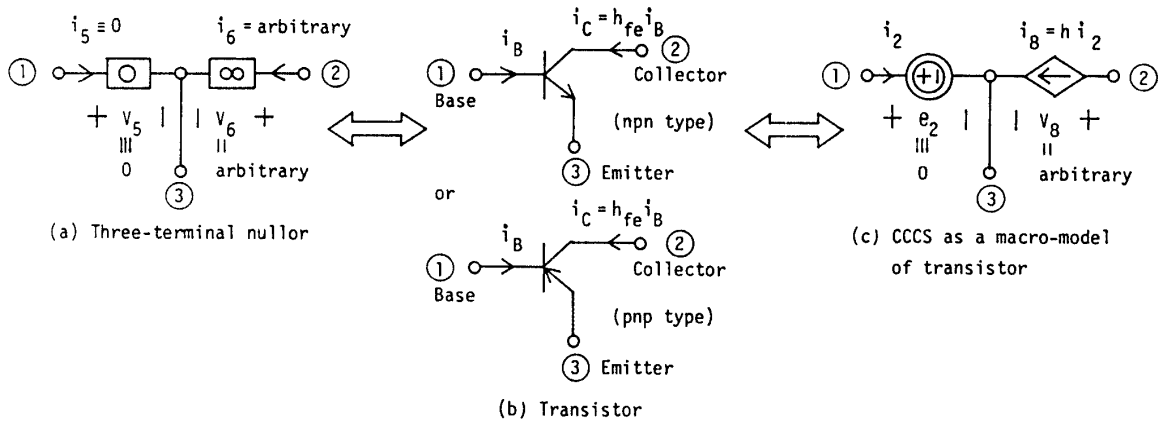

Fig. 1 Relation among nullor, transistor and CCCS.

$$\begin{bmatrix} W_1 \\ W_2 \\ W_3 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} \tag{1}$$

where

$$\left.\begin{aligned} &W_1 \triangleq [-i_1^T, \quad -v_0^T]^T, \quad X_1 \triangleq [e_1^T, \quad j_0^T]^T \\ &W_2 \triangleq -v_8, \quad X_2 \triangleq i_8 = KW_3 \\ &W_3 \triangleq i_2, \quad X_3 \triangleq -e_2 \equiv 0 \\ &K \triangleq \mathrm{diag}\,[h_1, h_2, \cdots, h_m], \quad h_i \geqq 0 \quad (i = 1 \sim m). \end{aligned}\right\} \tag{2}$$

In eq.(1), known vectors X_1 and X_3, unknown vectors W_1, W_2, W_3 and X_2, and submatrices of hybrid matrix $H_{11} \sim H_{33}$, in which every matrix-element is real, are used. The (i, j) element of transfer matrix $-H_{32}$ represents the current transfer ratio from the j-th controlled-current-source to the i-th current-sensor, where i, j $= 1 \sim m$. The coefficient matrix K is a real diagonal matrix. The (i,i) element of K is the current gain h_i of the i-th CCCS (i.e., the i-th transistor).

Equations (1) and (2) give the solution

$$\left.\begin{aligned} X_2 &= [F_d^{-1} \; KH_{31}]X_1 \\ W_1 &= [H_{11} + H_{12}F_d^{-1} \; KH_{31}]X_1 \\ W_2 &= [H_{21} + H_{22}F_d^{-1} \; KH_{31}]X_1 \\ W_3 &= [H_{31} + H_{32}F_d^{-1} \; KH_{31}]X_1 \end{aligned}\right\} \tag{3}$$

if the return difference matrix [14]

$$F_d \triangleq 1 - KH_{32} \tag{4}$$

is nonsingular (i.e., det $F_d \neq 0$).

From eq. (3), the following Lemma holds.

[Lemma 2] (i) The network $\mathcal{N}$ has a unique solution. $\Longleftrightarrow$ (ii) ① The matrix F_d is

nonsingular, if all h_i's take finite values, or ② All elements of the matrix $F_d^{-1}K$ are finite, if all h_i's may take infinite values and/or finite values.

[Lemma 3] (i) The nullator-norator-modeled resistive network N has a unique solution. $\Longleftrightarrow$ (ii) The transfer matrix $-H_{32}$ for the controlled-source-modeled resistive network N is nonsingular.

This proof is to be referred to Theorem 1 in literature [13].

The determinant of the return difference matrix F_d is expressed as

$$\begin{aligned}\det F_d = 1 &+ \{a_1h_1 + a_2h_2 + a_3h_3 + \cdots\cdots + a_{m-1}h_{m-1} + a_mh_m\} \\ &+ \{a_{m+1}h_1h_2 + a_{m+2}h_1h_3 + \cdots\cdots + a_{m(m+1)/2}h_{m-1}h_m\} + \cdots\cdots \\ &+ \{a_{l-m}h_1h_2\cdots h_{m-1} + a_{l-m+1}h_1h_2\cdots h_{m-2}h_m + \cdots + a_{l-1}h_2h_3\cdots h_m\} + a_lh_1h_2\cdots h_m \quad (5)\end{aligned}$$

where

$$l \triangleq \sum_{i=1}^{m} {}_mC_i = 2^m - 1 \quad (6)$$

$$\text{The coefficient of } h_{i_1}h_{i_2}\cdots h_{i_n} \triangleq \det\left[-H_{32}\begin{pmatrix} i_1 & i_2\cdots i_n \\ i_1 & i_2\cdots i_n \end{pmatrix}\right] \quad (7)$$

$$a_l \triangleq \det[-H_{32}] = (-1)^m \det H_{32} \neq 0. \quad (8)$$

The right-hand expression of eq. (7) is the principal minor [16] which consists of the i_1-, i_2-, $\cdots$, i_n-th rows and columns of matrix $-H_{32}$, where $1 \leqq i_1 < i_2 < \cdots < i_n \leqq m$, and $n = 1 \sim m$ [9]-[13].

2.3 DC Stability of Realization Circuit Using Transistors

The physical meanings that a realized transistor circuit is unstable, are as follows: (1) One or more transistors are cut-off and/or saturated, or (2) the transistor circuit is oscillating.

Stability of realization circuit is classified into five types [13], according to the activation process for practical electronic devices (i.e., transistors, etc.) and the region of their attainable gains. But in this paper, the DC gains of transistors are assumed to be finite maximum values, because of the aim of derivation of a fundamental criterion for stability (i.e., Theorem 1). The following discussion is performed in the complex-frequency domain (i.e., s-domain).

Actual transistors possess the phase-lag characteristics. Their characteristics are approximated by the first-order phase-lag characteristics as

$$\tilde{h_i}(s) \triangleq h_i/(1+sT_i), \quad h_i > 0, \quad T_i > 0 \quad (i = 1 \sim m), \quad (9)$$

where h_i is the finite DC gain of the i-th CCCS (i.e., the i-th transistor), s is the complex-frequency, and T_i is the time constant of the i-th CCCS (i.e., the i-th transistor).

The return difference matrix for the controlled-source-modeled resistive network $\mathcal{N}$ in which CCCS's possess the first-order phase-lag characteristics is defined as

$$\tilde{F}_d(s) \triangleq 1 - \tilde{K}(s)\, H_{32} \tag{10}$$

where

$$\tilde{K}(s) \triangleq \text{diag}\,[\tilde{h}_1(s),\ \tilde{h}_2(s),\cdots\cdots,\ \tilde{h}_m(s)]. \tag{11}$$

Its determinant is expressed as

$$\det \tilde{F}_d(s) = \frac{s^m b_m + s^{m-1} b_{m-1} + \cdots\cdots + s^1 b_1 + s^0 b_0}{(1+sT_1)(1+sT_2)\cdots\cdots(1+sT_m)} \tag{12}$$

where

$$\left.\begin{aligned} b_m &\triangleq T_1 T_2 \cdots T_m > 0 \\ b_{m-1} &\triangleq \sum_{i=1}^{m} (1+a_i h_i) T_1 T_2 \cdots T_m / T_i \\ b_0 &\triangleq \det F_d. \end{aligned}\right\} \tag{13}$$

In eq.(13), b_0 is equal to eq.(5). Stability of the network $\mathcal{N}$ depends on the location of the zeros of $\det \tilde{F}_d(s)$. From the Hurwitz criterion [17], the following Lemma holds.

[Lemma 4] (i) The network $\mathcal{N}$ is asymptotically stable. $\Longrightarrow$ (ii) In eq. (12), $b_m > 0$, $b_{m-1} > 0, \cdots\cdots, b_0 > 0$.

[Definition 3] The netwok $\mathcal{N}$ is DC stable, if $\mathcal{N}$ is asymptotically stable only when every $T_i \to 0_+$.

[Theorem 1] (i) The network $\mathcal{N}$ is asymptotically stable. $\Longrightarrow$ (ii) The network $\mathcal{N}$ is DC stable. $\Longleftrightarrow$ (iii) $\det F_d > 0$. $\Longrightarrow$ (iv) $a_l > 0$.

(Proof) (i) $\Rightarrow$ (ii): It is obvious from Definition 3.

(ii) $\Rightarrow$ (iii): Since $\mathcal{N}$ is DC stable, $\mathcal{N}$ has a unique solution. Hence, from Lemma 2, the matrix F_d is nonsingular, i.e., $\det F_d \neq 0$, because of the assumption that every h_i is finite. If $\det F_d < 0$, eq. (12) possess the zeros in the closed-right-half s-plane, because $b_m \to 0_+$ when every $T_i \to 0_+$. Then $\mathcal{N}$ is not DC stable, which is a contradiction. Hence, the proposition is true.

(iii) $\Rightarrow$ (ii) : The converse in the above proof is also true.

(iii) $\Rightarrow$ (iv) : From Lemma 3, $a_l = \det[-H_{32}] \neq 0$ in eqs. (5) and (8). Hence, the condition $\det F_d > 0$ for sufficiently large h_i's leads to $a_l > 0$. (Q.E.D.)

Therefore, it is necessary to find the nullator-norator pairs such that the condition $\det F_d > 0$ (at least, $a_l > 0$) is satisfied in the controlled-source-modeled resistive network $\mathcal{N}$, for getting a stable realization circuit using transistors from a given nullator-norator-

modeled resistive network N.

3. Example Circuit

3.1 Example Circuit and Its Stability Analysis

Fig. 2(a) shows a nullator-norator-modeled resistive network N such that the realization circuit using transistors is stable or unstable, according to the selection of pairs of nullators and norators. The gain of this circuit (Fig. 2(a)) is expressed as

$$\text{Gain}_{\text{Nullor}} \triangleq V_{out}/e_1 = -R_{c2}\{(R_1+R_2+R_{c1})R_e+R_2R_{c1}\}/R_2R_eR_{c1} < 0. \tag{14}$$

Tow ways (Case 1, Case 2) exist in replacing nullators and norators in Fig. 2(a) with transistors. One way (case 1) is that nullator 1 and norator 1 construct transistor Q_1, and nullator 2 and norator 2 construct transistor Q_2 as shown in Fig. 2(c). The other way (Case 2) is that nullator 2 and norator 1 construct transistor Q_1, and nullator 1 and norator 2 construct transistor Q_2 as shown in Fig. 2(d). In Figs. 2(c) and (d), transistors are represented with npn type, for convenience.

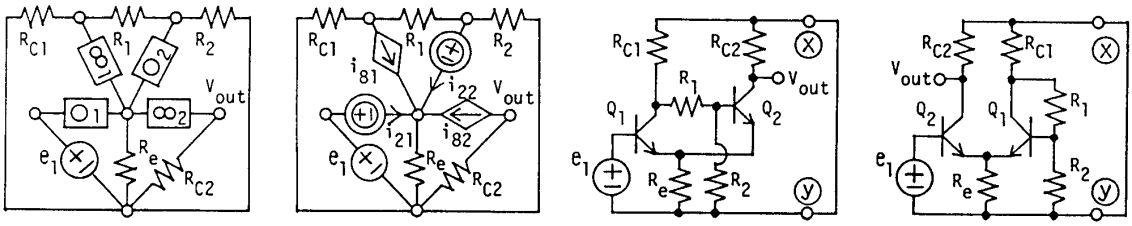

Fig. 2　Circuits for example.

[Case 1 (Q_1 : Nu_1-No_1, Q_2 : Nu_2-No_2)]

In the controlled-source-modeled resistive network $\mathcal{N}$ of Fig. 2(b),

$$i_{81}=h_1i_{21}, \qquad i_{82}=h_2i_{22} \tag{15}$$

$$-H_{32}=\begin{matrix} \\ -i_{21} \\ -i_{22} \end{matrix}\begin{matrix} \overset{i_{81}}{} \\ \begin{bmatrix} R_1/(R_1+R_{c1}) & 1 \\ R_{c1}/(R_1+R_{c1}) & 0 \end{bmatrix} \end{matrix}\begin{matrix} \overset{i_{82}}{} \\ \end{matrix}, \quad K=\begin{bmatrix} h_1 & 0 \\ 0 & h_2 \end{bmatrix}. \tag{16}$$

$$\therefore \det F_d \triangleq \det[1-KH_{32}]=\det\begin{bmatrix} 1+R_1h_1/(R_1+R_{c1}) & h_1 \\ R_{c1}h_2/(R_1+R_{c1}) & 1 \end{bmatrix}$$

$$=1+R_1h_1/(R_1+R_{c1})-R_{c1}h_1h_2/(R_1+R_{c1}) \tag{17}$$

$$\therefore a_l=-R_{c1}/(R_1+R_{c1})<0, \quad l \triangleq 3. \tag{18}$$

From Theorem 1, this realization circuit of Fig. 2(c) is unstable ($\because$ det $F_d<0$ for sufficiently large h_1 and h_2), and therefore this circuit does not simulate the original nullator-norator circuit of Fig. 2(a).

[Case 1' (Q_1: Nu_1-No_1, Q_2: Nu_2-No_2)]

If current gains h_1 and h_2 are relatively small, and the condition det $F_d>0$ is satisfied, then the realization circuit of Fig. 2(c) is stable, but does not simulate the original nullator-norator circuit of Fig. 2(a). Therefore, this case is nonsense in the situation that the larger the current gains, the better the realization circuit must simulate the original nullator-norator circuit. However, this case is interesting in the sense of uniqueness of solution for the transistor circuit with positive feedback.

Modifying the condition det $F_d>0$ leads as follows:

$$\det F_d=1+R_1h_1/(R_1+R_{c1})-R_{c1}h_1h_2/(R_1+R_{c1})>0 \tag{19}$$

$$\therefore\ R_1>R_{c1}(h_1h_2-1)/(1+h_1)=R_{c1}h_2(1-\alpha_1/\alpha_2h_1) \tag{20}$$

where

$$\alpha_i \triangleq h_i/(1+h_i) \qquad (i=1,2). \tag{21}$$

Equation (20) corresponds to eq.(1) in literature [15]. The gain of this circuit (Fig. 2(c)) in the case of det $F_d>0$, is expressed as

$$\text{Gain}_{PF}\triangleq\frac{V_{out}}{e_1}=R_{c2}\left\{\left(\frac{1}{R_1+R_{c1}}+\frac{1}{R_2}\right)(h_1+1)h_2+\frac{R_{c1}h_1h_2}{(R_1+R_{c1})R_e}\right\}\Big/\left\{1+\frac{R_1h_1}{R_1+R_{c1}}-\frac{R_{c1}h_1h_2}{R_1+R_{c1}}\right\}. \tag{22}$$

[Case 2 (Q_1: Nu_2-No_1, Q_2: Nu_1-No_2)]

In Fig. 2(b),

$$i_{s1}=h_1i_{22},\quad i_{s2}=h_2i_{21} \tag{23}$$

$$-H_{32}=\begin{matrix}\\ -i_{22}\\ -i_{21}\end{matrix}\overset{\begin{matrix}i_{s1}\qquad\quad i_{s2}\end{matrix}}{\begin{bmatrix} R_{c1}/(R_1+R_{c1}) & 0\\ R_1/(R_1+R_{c1}) & 1\end{bmatrix}},\quad K=\begin{bmatrix} h_1 & 0\\ 0 & h_2\end{bmatrix}. \tag{24}$$

$$\therefore\det F_d\triangleq\det[1-KH_{32}]=\det\begin{bmatrix} 1+R_{c1}h_1/(R_1+R_{c1}) & 0\\ R_1h_2/(R_1+R_{c1}) & 1+h_2\end{bmatrix}$$

$$=1+R_{c1}h_1/(R_1+R_{c1})+h_2+R_{c1}h_1h_2/(R_1+R_{c1}). \tag{25}$$

For $h_1>0$ and $h_2>0$, the condition det $F_d>0$ is satisfied, that is, Theorem 1 is satisfied. For $T_1>0$ and $T_2>0$, det $\tilde{F}_d(s)$ of eq. (12) does not possess the zeros in the closed-right-half s-plane. Hence, this realization circuit of Fig. 2(d) is stable, and simulates the original nullator-norator circuit of Fig. 2(a). The gain of this circuit (Fig. 2(d)) is expressed as

$$\text{Gain}_{NF} \triangleq \frac{V_{out}}{e_1} = -R_{c2}\left\{\left(\frac{1}{R_1+R_{c1}}+\frac{1}{R_2}\right)(h_1+1)h_2+\frac{R_{c1}h_1h_2}{(R_1+R_{c1})R_e}+\frac{h_2}{R_e}\right\}\Big/\left\{1+\frac{R_{c1}h_1}{R_1+R_{c1}}+h_2+\frac{R_{c1}h_1h_2}{R_1+R_{c1}}\right\}. \quad (26)$$

3.2 Consideration on Bias Problem

It is necessary to give the bias in realizing the transistor circuits of Figs. 2(c) and (d), because they are the circuits in respect to the signal, i.e., the circuits without biasing. For example, if transistors Q_1 and Q_2 are npn type, and if one DC voltage supply is used, actual transistor circuits for Figs. 2(c) and (d) are obtained by the following manner: (1) The vertices ⓧ and ⓨ are separated, and (2) the vertex ⓨ is grounded, and (3) the vertex ⓧ is connected to a positive DC voltage supply. Then the circuit for Fig. 2(c) is a well-known Schmitt trigger [15].

Fig. 3 shows the realized transistor circuits with DC voltage supplies V_{s1}, V_{s2} and V_{s3} in the case where the input transistor is npn type. Table 1 shows the combination of DC voltage supplies. The suffix $j=0$ denotes the realized transistor circuits with one DC voltage supply, and the suffix $j=1,2$ denotes the realized transistor circuits with two DC voltage supplies.

In Fig. 3, the input voltage is e_1, and the output voltage is V_{out}, and the collector voltages of transistors Q_1 and Q_2 are V_{c1} and V_{c2} respectively, therefore, $V_{out}=V_{c2}$. For the used resistors in Case 1 and Case 2, the gain of the original nullator-norator circuit of Fig. 2(a) is evaluated by eq. (14) as

$$\text{Gain}_{Nullor} = -0.813 < 0. \quad (27)$$

3.3 Experimental Results

The experimental results of the realized transistor circuits of Fig. 3 are shown in Figs. 4 and 5 and Tables 2 and 3. The input voltage e_1 is varied from 0 V (DC) to +10 V (DC), and from +10 V (DC) to 0 V (DC). The collector voltages (DC), the base voltages (DC) and the emitter voltages (DC) of transistors Q_1 and Q_2 are measured.

[Experimental results using one DC voltage supply]

Fig. 4 and Table 2 show the experimental results of the realized transistor circuits with one DC voltage supply.

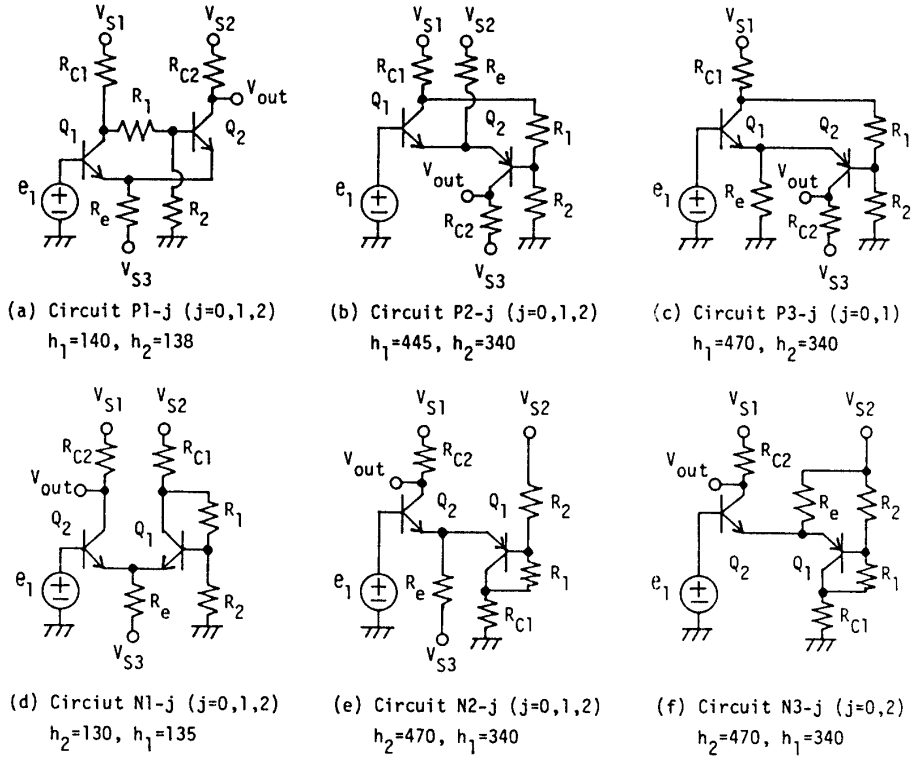

Fig. 3 Realized transistor circuits with DC voltage supplies.
- (a), (b), (c) : Case 1 (Positive feedback, det $F_d<0$)
- (d), (e), (f) : Case 2 (Negative feedback, det $F_d>0$)
- $R_{c1}=4.2k\Omega$, $R_{c2}=1.0k\Omega$, $R_e=3.0k\Omega$, $R_1=2.0k\Omega$, $R_2=6.1k\Omega$
- (a), (d) : npn : 2SC732
- (b), (c), (e), (f) : npn : 2SC1222, pnp : 2SA640
- h_i : Current gain of transistor Q_i (i=1,2)

Table 1. Combination of DC voltage supplies for the circuits of Fig. 3.

j	V_{s1}	V_{s2}	V_{s3}
0	+10V	+10V	0 V (ground)
1	+10V	+10V	−5 V
2	+10V	+ 5 V	0 V (ground)

Figs. 4(a)~(c) show the following : The circuits for Case 1 are unstable and do not simulate the original nullator-norator circuit of Fig. 2(a), because one or two transistors are cut-off and/or saturated, that is, there is no region such that both the transistors Q_1 and Q_2 operate linearly. These realized transistor circuits exhibit the hysteresis characteristics.

Figs. 4(a')~(c') show the following : The circuits for Case 1' are stable but do not

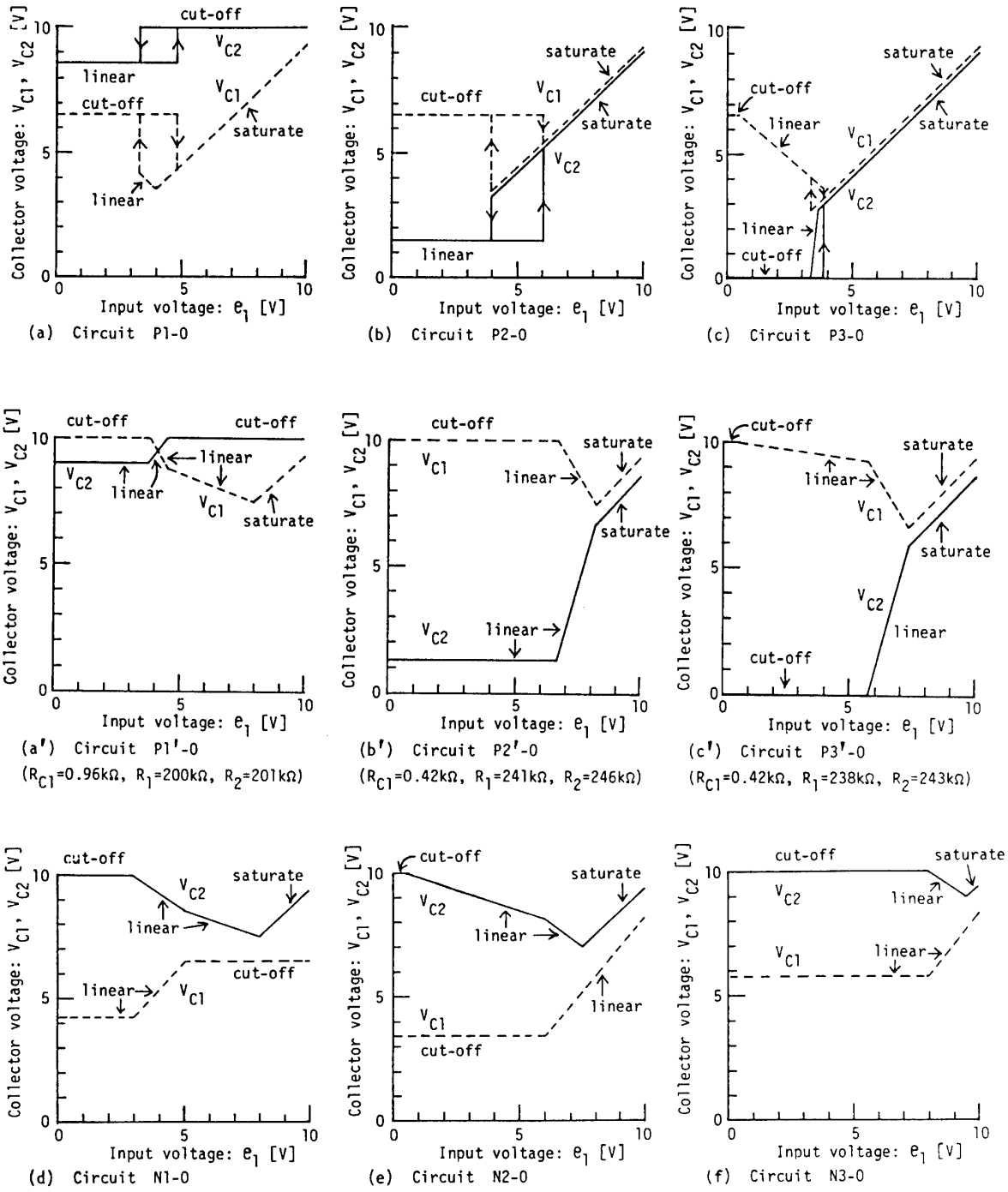

Fig. 4　DC characteristics of the realized transistor circuits with one DC voltage supply. (Temperature : Ta=17℃, $V_{out}=V_{c2}$)
(a), (b), (c) :　Case 1　(Positive feedback,　det $F_d<0$)
(a′), (b′), (c′) :　Case 1′　(Positive feedback,　det $F_d>0$)
(d), (e), (f) :　Case 2　(Negative feedback,　det $F_d>0$).

Table 2. Experimental results using one DC voltage supply.

Fig. 4/Circuit	Input voltage range that both the transistors operate linearly	Measured gain Gain $\triangleq \triangle V_{out}/\triangle e_1$	(Theoretical gain by eqs.(22),(26))
(a')/P1'-0	$e_1=3.8-4.5$ V	1.905	(4.671)
(b')/P2'-0	$e_1=6.7-8.2$ V	3.878	(7.320)
(c')/P3'-0	$e_1=5.7-7.3$ V	4.540	(7.550)
(d)/N1-0	$e_1=3.0-5.0$ V	−0.775	(−0.806)
(e)/N2-0	$e_1=6.0-7.6$ V	−0.790	(−0.811)
(f)/N3-0	$e_1=8.0-9.5$ V	−0.796	(−0.811)

simulate the original nullator-norator circuit of Fig. 2(a), because the measured gains are positive in the region of linear operation. As shown in Table 2, the measured gains are small in comparison with the theoretical gains which are evaluated by eq.(22). This is because eq.(22) (and also eq.(26)) is derived under the assumption that the base-resistances and the emitter-resistances are zero, and the collector-resistances are infinite in all transistors.

Figs. 4(d)~(f) show the following: The circuits for Case 2 are stable and simulate the original nullator-norator circuit of Fig. 2(a), because the measured gains are approximately equal to the gain of nullator-norator circuit (−0.813).

Hence, the experimental results (Case 1, Case 1', Case 2) using one DC voltage supply agree with the stability analysis described in section 3.1.

[Experimental results using two DC voltage supplies]

Fig. 5 and Table 3 show the experimental results of the realized transistor circuits with two DC voltage supplies. Figs. 5 (a1)~(c1) show that the circuits for Case 1 are unstable and do not simulate the original nullator-norator circuit of Fig. 2(a). These realized transistor circuits exhibit the hysteresis characteristics. Figs. 5 (d1)~(f1) show that the circuit for Case 2 are stable and simulate the original nullator-norator circuit of Fig. 2(a) in the region that both the transistors Q_1 and Q_2 operate linearly. Hence, the experimental results (Case 1, Case 2) using two DC voltage supplies agree with the stability analysis described in section 3.1.

In the case where the input transistor is pnp type, the experimental results are in complementary relation to the above experimental results.

4. Conclusion

The stability problem in replacing nullators and norators of a nullator-norator -modeled resistive network with transistors, has been investigated. The realized tran-

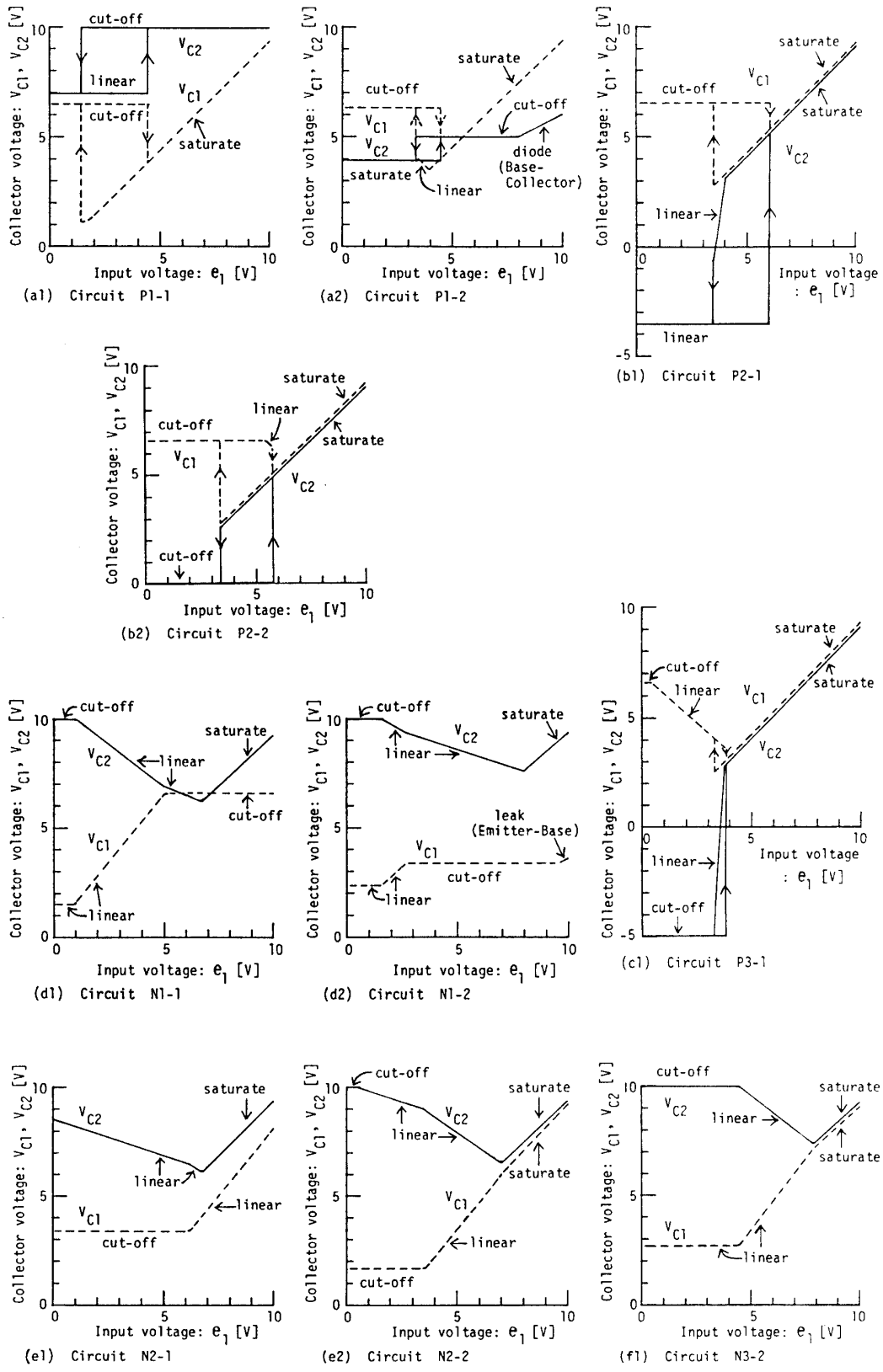

Fig. 5　DC characteristics of the realized transistor circuits with two DC voltage supplies. (Temperature : Ta＝22℃, $V_{out}=V_{c2}$)
(a1), (a2), (b1), (b2), (c1) : Case 1 (Positive feedback, det $F_d<0$)
(d1), (d2), (e1), (e2), (f1) : Case 2 (Negative feedback, det $F_d>0$).

Table 3. Experimental results using two DC voltage supplies.

Fig. 5/Circuit	Input voltage range that both the transistors operate linearly	Measured gain Gain $\triangleq \triangle V_{out}/\triangle e_1$	(Theoretical gain by eqs.(22),(26))
(d1)/N1-1	$e_1 = 1.0 - 5.2$ V	−0.789	(−0.806)
(d2)/N1-2	$e_1 = 1.6 - 2.7$ V	−0.725	(−0.806)
(e1)/N2-1	$e_1 = 6.2 - 6.8$ V	−0.737	(−0.811)
(e2)/N2-2	$e_1 = 3.5 - 7.0$ V	−0.792	(−0.811)
(f1)/N3-2	$e_1 = 4.3 - 7.9$ V	−0.777	(−0.811)

sistor circuits of Fig. 3 for the example nullator-norator circuit of Fig. 2(a) operate stably or unstably, according to the selection of pairs of nullators and norators. Those experimental results (Figs. 4 and 5, Tables 2 and 3) agree with the stability analysis, which is based on the return difference matrix F_d. The stability criterion, which is given by Theorem 1, is useful in the realization of nullator-norator-modeled resistive network with various practical electronic devices, especially transistors.

The bias problem, which has been considered briefly in section 3.2, is left to be studied.

References

[1] Y. Oono, "Formal realizability of linear networks", Proc. Symp. on Active Networks and Feedback Systems, Polytechnic Press of the Polytechnic Inst. of Brooklyn, Brooklyn, N.Y., April 1960.

[2] H.J. Carlin and D.C. Youla, "Network synthesis with negative resistors", Proc. IRE, vol. 49, pp. 907-920, May 1961.

[3] H.J. Carlin, "Singular network elements", IEEE Trans. on Circuit Theory, vol. CT-11, pp. 67-72, March 1964.

[4] Y. Kato and T. Matsumoto, "Synthesis of Wien-bridge type operational amplifier oscillator circuits based on the nullator-norator equivalent transformations, and their experiments", Convention Records of Hokuriku section of I.E.E.I.T. of Japan, B-30, Oct. 1983 (in Japanese), and "Synthesis of Wien-bridge type op-amp oscillator circuits by using equivalent circuit transformations in nullator-norator-modeled circuit", Trans. IECE of Japan, vol. J68-A, no. 4, pp. 414-415, April 1985 (in Japanese).

[5] T. Matsumoto and Y. Kato, "Existence of unique solutions and the state equations for linear active networks containing singular network elements", Trans. IECE of Japan, vol. J57-A, no. 8, pp. 629-630, Aug. 1974 (in Japanese).

[6] Y. Kato, "Realization of arbitrary 2×2 conductance matrix using two operational amplifiers", Memoirs of the Fukui Institute of Technology, no. 12, pp. 9-28, Oct. 1982.

[7] T. Yanagisawa and N. Kambayashi, "Realization of arbitrary conductance matrix using operational amplifiers", Trans. IECE of Japan, vol. J59-A, no. 5, pp. 401-408, May 1976 (in Japanese).

[8] A. Antoniou, "Realisation of gyrators using operational amplifiers, and their use in RC-active-notwork synthesis", Proc. IEE, vol. 116, no. 11, pp. 1838-1850, Nov. 1969.

[9] N. Fujii, "DC stability of nullator-norator circuits realized with operational amplifiers", Trans. IECE of Japan, vol. E61, no. 8, pp. 625-630, Aug. 1978.

[10] Y. Kato and T. Matsumoto, "DC stability of nullator-norator-modeled resistive networks realized with practical electronic devices of nullors", Paper of Technical Group, TGCAS80-14, IECE of Japan, May 1980 (in Japanese).

[11] Y. Kato and T. Matsumoto, "Stability of nullator-norator-modeled resistive notworks realized with transistors", Convention Records of Hokuriku section of I.E.E.I.T. of Japan, B-20, Oct. 1981 (in Japanese), and Trans. IECE of Japan, vol. J64-A, no. 12, pp. 1054-1055, Dec. 1981 (in Japanese).

[12] Y. Kato and T. Matsumoto, "Experimental research on the realization of nullator-norator-modeled network using operational amplifiers", Paper of Technical Group, TGCAS83-24, June 1983 (in Japanese).

[13] Y. Kato and T. Matsumoto, "DC stability of nullator-norator-modeled resistive networks realized with practical electronic devices", Trans. IECE of Japan, vol. J67-A, no. 7, pp. 666-673, July 1984 (in Japanese).

[14] L.O. Chua and P-M. Lin, "Computer-aided analysis of electronic circuits: Algorithms and computational techniques", chap. 6, Prentice-Hall, Englewood Cliffs, New Jersey, 1975.

[15] R.O. Nielsen and A.N. Willson, Jr., "Topological criteria for establishing the uniqueness of solutions to the DC equations of transistor networks", IEEE Trans. on Circuits and Systems, vol. CAS-24, no. 7, pp. 349-362, July 1977.

[16] S. Kodama and N. Suda, "Matrix theory for system control", p. 32, Keisoku-jido-seigyo-gakkai, Tokyo, 1978 (in Japanese).

[17] W-K. Chen, "Active network and feedback amplifier theory", chap. 6, Hemisphere Publishing Corporation, McGraw-Hill Book Company, New York, 1980.