Realization of Arbitrary 2×2 Conductance Matrix Using Two Operational Amplifiers

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Abstract — Three types of circuits for the realization of arbitrary 2×2 conductance matrix using nullators and norators are derived systematically by Yanagisawa and Kambayashi's method. One of them is a new proposed circuit. These nullator-norator circuits are applied to the design of impedance-matched bilateral amplifiers using operational amplifiers and resistors. Their experimental results are also shown. Stability is checked by using the return difference matrix.

I. Introduction

The nullator is a two-terminal element for which both terminal current and terminal voltage are zero, and the norator is a two-terminal element for which terminal current and terminal voltage are arbitrary and can independently take any values (Fig. 1). The nullator-norator pair is termed the nullor, and corresponds to some physical devices such as operational amplifier, transistor, FET, etc. Specially, IC operational amplifier is excellent in cost and performance. Nullators and norators are commonly used in the electronic circuit analysis and synthesis [1]-[7].

Recently, two circuits for the realization of arbitrary 2×2 conductance matrix using two operational amplifiers were proposed. One is Yanagisawa and Kambayashi's circuit (TYPE I) which is based on the row- and column-manipulation for the admittance matrix [2], and the other is Imai et al's circuit (TYPE II) which is based on the concept of Negative Impedance Converter [7].

In this paper, a new circuit (TYPE III) for that is presented, and it is shown that these circuits (TYPE I, TYPE II, TYPE III) can be derived systematically by Yanagisawa and Kambayashi's method [2]. These circuits are applied to the impedance-matched bilateral amplifiers realized with operational amplifiers and resistors, and their experimental results are also shown. Stability is checked by using the return difference matrix [8]-[11].

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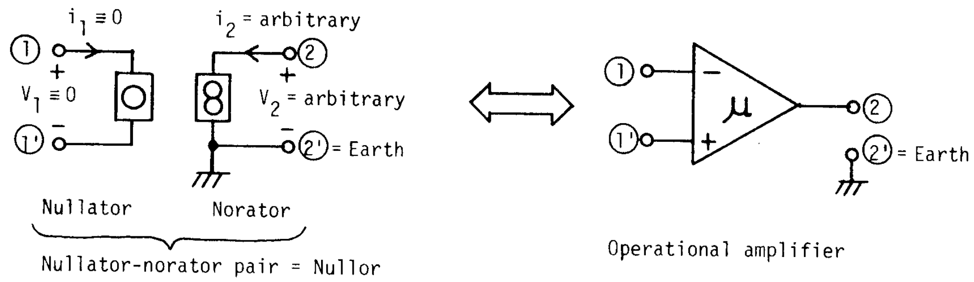


Fig. 1.　Nullor and operational amplifier.

2.　Realization of Arbitrary 2×2 Conductance Matrix Using Nullators and Norators

A two-port network shown in Fig. 2 is written by using the (short-circuit) admittance matrix Y as

$$I = YV \tag{1}$$

or

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{2}$$

If nullators and norators as active elements and resistors as passive elements are used, all matrix elements $Y_{11}-Y_{22}$ are real, and the admittance matrix is called "the conductance matrix".

In this section, three types of circuits for the realization of arbitrary 2×2 conductance matrix are derived systematically by using Yanagisawa and Kambayashi's method. The term "arbitrary" means that all matrix elements $Y_{11}-Y_{22}$ can take any values of plus, minus and zero independently.

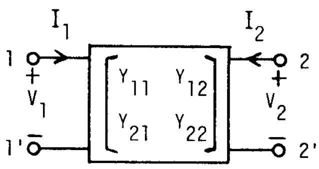


Fig. 2.　Two-port network.

2.1　Derivation of TYPE I Circuit (Yanagisawa and Kambayashi's method)

Yanagisawa and Kambayashi proposed a method for the realization of arbitrary 2×2 conductance matrix using nullators and norators [2]. This method is based on the row- and column-manipulation for the admittance matrix. In this subsection and following subsections 2.2 and 2.3, the following assumptions are required.

(Assumption 1)　Two operational amplifiers, i.e. two nullator-norator pairs, are used for the realization of 2×2 admittance matrix.

(Assumption 2) Norators are grounded, because the (grounded-output type) operational amplifiers are used (Fig. 1).

(Assumption 3) All resistors are connected only at the terminals of nullators and norators.

(Assumption 4) Port-terminals are taken at the nodes connected by nullators.

[Yanagisawa and Kambayashi's method]

(Step 1) A passive network in which all nullators and norators are removed (i.e. open-circuited) is written by the following 6×6 admittance matrix representation

$$\begin{array}{c} \\ ① \\ ② \\ ③ \\ ④ \\ ⑤ \\ ⑥ \end{array}\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix} = \begin{array}{c} \begin{array}{cccccc} ① & ② & ③ & ④ & ⑤ & ⑥ \end{array} \\ \begin{bmatrix} y_{11} & -y_{12} & -y_{13} & -y_{14} & -y_{15} & -y_{16} \\ -y_{12} & y_{22} & -y_{23} & -y_{24} & -y_{25} & -y_{26} \\ -y_{13} & -y_{23} & y_{33} & -y_{34} & -y_{35} & -y_{36} \\ -y_{14} & -y_{24} & -y_{34} & y_{44} & -y_{45} & -y_{46} \\ -y_{15} & -y_{25} & -y_{35} & -y_{45} & y_{55} & -y_{56} \\ -y_{16} & -y_{26} & -y_{36} & -y_{46} & -y_{56} & y_{66} \end{bmatrix} \end{array} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} \tag{3}$$

where the notation ⓘ $(i=1,2,\cdots,6)$ denotes the node number. This admittance matrix is symmetric and its elements satisfy the relations

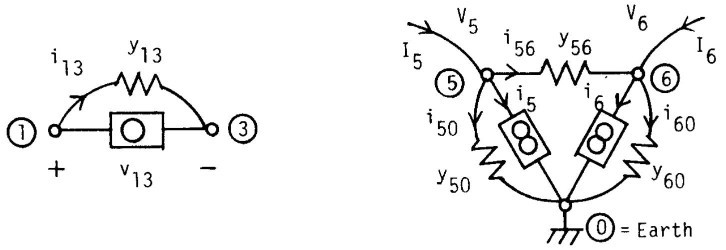
$$y_{ii}=\sum_{\substack{j=0\\ j\neq i}}^{6} y_{ij},\quad y_{ij}\geqq 0,\quad \text{for } i=1,2,\cdots,6 \tag{4}$$

because of passive network.

(Step 2) Two nullators are inserted to the nodes ①-③ and ②-④, and two norators are inserted to the nodes ⑤-⓪ and ⑥-⓪, where the notation ⓪ denotes the reference node, i.e. earth terminal.

In Fig. 3(a), the voltage of branch y_{13} is zero because of the inserted nullator, and hence its current is also zero. That is, the electric behavior at nodes ① and ③ is the same whether the branch y_{13} exists or not. Therefore, the branch y_{13} is removed $(y_{13}=0)$. For the same reason, the branch y_{24} is removed $(y_{24}=0)$, too.

In Fig. 3(b), if the node voltages V_5 and V_6 are given, the branch currents flow as $i_{50}=y_{50}V_5$, $i_{60}=y_{60}V_6$ and $i_{56}=y_{56}(V_5-V_6)$, but the node currents I_5 and I_6 are arbitrary because the norator currents i_5 and i_6 are arbitrary. If the node currents I_5 and I_6 are given, the branch currents i_{50}, i_{60} and i_{56} are arbitrary because of the inserted norators, therefore the node voltages $V_5=y_{50}^{-1}i_{50}$ and $V_6=y_{60}^{-1}i_{60}$ are arbitrary. Similarly, if I_5 (V_5) and V_6 (I_6) are given, V_5 (I_5) and I_6 (V_6) are arbitrary. That is, the electric behavior at nodes ⑤ and ⑥ is the same whether the branches y_{50}, y_{60} and y_{56} exist or not. Therefore, the branches y_{50}, y_{60} and y_{56} are removed ($y_{50}=y_{60}=y_{56}=0$).



(a) Effect of inserted nullator ($v_{13} \equiv 0$)

(b) Effect of inserted norator (i_5, i_6 : arbitrary)

Fig. 3. Effects of the insertions of nullator and norator.

Now, Eq. (3) is rewritten as

$$\begin{array}{cc} & \begin{array}{cccccc} \text{①} & \text{②} & \text{③} & \text{④} & \text{⑤} & \text{⑥} \end{array} \\ \begin{array}{c} \text{①} \\ \text{②} \\ \text{③} \\ \text{④} \\ \text{⑤} \\ \text{⑥} \end{array} & \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix} = \begin{bmatrix} y_{11} & -y_{12} & 0 & -y_{14} & -y_{15} & -y_{16} \\ -y_{12} & y_{22} & -y_{23} & 0 & -y_{25} & -y_{26} \\ 0 & -y_{23} & y_{33} & -y_{34} & -y_{35} & -y_{36} \\ -y_{14} & 0 & -y_{34} & y_{44} & -y_{45} & -y_{46} \\ -y_{15} & -y_{25} & -y_{35} & -y_{45} & y_{55} & 0 \\ -y_{16} & -y_{26} & -y_{36} & -y_{46} & 0 & y_{66} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix}. \end{array} \qquad (5)$$

The inserted nullators restrict the node voltages as $V_1=V_3$ and $V_2=V_4$. Therefore, the columns ③ and ④ are added to the columns ① and ②, respectively. The node currents I_5 and I_6 are arbitrary because of the inserted norators. Therefore, the rows ⑤ and ⑥ are deleted. The nodes ③ and ④ are internal nodes, therefore, $I_3=I_4=0$.

Equation (5) is reduced to the following 4×4 matrix representation

$$\begin{array}{cc} & \begin{array}{cccc} \text{①}=\text{③} & \text{②}=\text{④} & \text{⑤} & \text{⑥} \end{array} \\ \begin{array}{c} \text{①} \\ \text{②} \\ \text{③} \\ \text{④} \end{array} & \begin{bmatrix} I_1 \\ I_2 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} y_{11} & -(y_{12}+y_{14}) & -y_{15} & -y_{16} \\ -(y_{12}+y_{23}) & y_{22} & -y_{25} & -y_{26} \\ y_{33} & -(y_{23}+y_{34}) & -y_{35} & -y_{36} \\ -(y_{14}+y_{34}) & y_{44} & -y_{45} & -y_{46} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_5 \\ V_6 \end{bmatrix}. \end{array} \qquad (6)$$

(Step 3) Equation (6) is reduced to the 2×2 matrix representation which expresses the two-port characteristics.

Choosing the admittances

$$y_{14}=y_{23}=y_{34}=0 \qquad (7)$$

in eq.(6) without loss of generality, the following expression is obtained

$$
\begin{array}{c c c}
 & & \begin{array}{cccc} ①=③ & ②=④ & ⑤ & ⑥ \end{array} \\
\begin{array}{c} ① \\ ② \\ ③ \\ ④ \end{array} \begin{bmatrix} I_1 \\ I_2 \\ 0 \\ 0 \end{bmatrix} & = & \begin{bmatrix} y_{11} & -y_{12} & -y_{15} & -y_{16} \\ -y_{12} & y_{22} & -y_{25} & -y_{26} \\ y_{33} & 0 & -y_{35} & -y_{36} \\ 0 & y_{44} & -y_{45} & -y_{46} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_5 \\ V_6 \end{bmatrix}
\end{array}
\qquad (8)
$$

From the rows ③ and ④,

$$
\left.
\begin{aligned}
V_5 &= (y_{33}y_{46}V_1 - y_{36}y_{44}V_2)/\triangle \\
V_6 &= (-y_{33}y_{45}V_1 + y_{35}y_{44}V_2)/\triangle \\
\triangle &\triangleq y_{35}y_{46} - y_{36}y_{45}.
\end{aligned}
\right\} \qquad (9)
$$

Substituting eq.(9) into the rows ① and ② in eq.(8), the final 2×2 admittance matrix representation is obtained as

$$
\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad (10)
$$

where

$$
\left.
\begin{aligned}
Y_{11} &\triangleq y_{11} - y_{33}(y_{15}y_{46} - y_{16}y_{45})/\triangle \\
&= (y_{10} + y_{12} + y_{15} + y_{16}) - (y_{30} + y_{35} + y_{36})(y_{15}y_{46} - y_{16}y_{45})/(y_{35}y_{46} - y_{36}y_{45}) \\
Y_{12} &\triangleq -y_{12} - y_{44}(y_{16}y_{35} - y_{15}y_{36})/\triangle \\
&= -y_{12} - (y_{40} + y_{45} + y_{46})(y_{16}y_{35} - y_{15}y_{36})/(y_{35}y_{46} - y_{36}y_{45}) \\
Y_{21} &\triangleq -y_{12} - y_{33}(y_{25}y_{46} - y_{26}y_{45})/\triangle \\
&= -y_{12} - (y_{30} + y_{35} + y_{36})(y_{25}y_{46} - y_{26}y_{45})/(y_{35}y_{46} - y_{36}y_{45}) \\
Y_{22} &\triangleq y_{22} - y_{44}(y_{26}y_{35} - y_{25}y_{36})/\triangle \\
&= (y_{20} + y_{12} + y_{25} + y_{26}) - (y_{40} + y_{45} + y_{46})(y_{26}y_{35} - y_{25}y_{36})/(y_{35}y_{46} - y_{36}y_{45}).
\end{aligned}
\right\} \qquad (11)
$$

The matrix elements $Y_{11} - Y_{22}$ can take arbitrary values independently, because they have plus- and minus-terms and many freedoms. Therefore, whenever any 2×2 admittance matrix is given, the admittance values y_{ij}'s can be always determined by equating it to eqs.(10),(11).

The nullator-norator circuit for eq.(10) is shown in Fig.4. This is the original circuit proposed by Yanagisawa and Kambayashi [2].

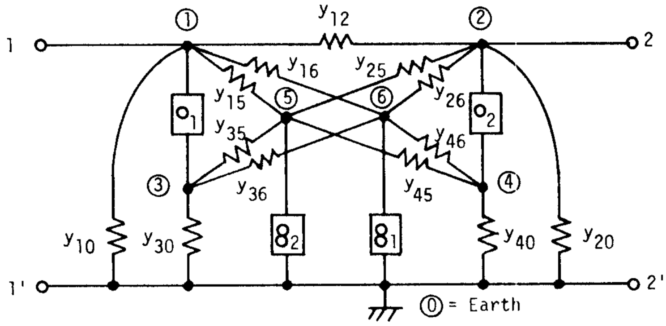


Fig. 4. TYPE I circuit for the realization of arbitrary 2×2 conductance matrix.

2.2 Derivation of TYPE II Circuit

Another circuit for the realization of arbitrary 2×2 conductance matrix can be derived by choosing another set of admittance values in step 3 in Yanagisawa et al's original method.

(Step 3′) Choosing the admittances

$$y_{14}=y_{16}=y_{23}=y_{25}=y_{36}=y_{45}=0 \qquad (12)$$

in eq.(6) without loss of generality, the following expression is obtained

$$\begin{array}{c} \\ ① \\ ② \\ ③ \\ ④ \end{array}\begin{bmatrix} I_1 \\ I_2 \\ 0 \\ 0 \end{bmatrix} = \begin{array}{c} \begin{array}{cccc} ①=③ & ②=④ & ⑤ & ⑥ \end{array} \\ \begin{bmatrix} y_{11} & -y_{12} & -y_{15} & 0 \\ -y_{12} & y_{22} & 0 & -y_{26} \\ y_{33} & -y_{34} & -y_{35} & 0 \\ -y_{34} & y_{44} & 0 & -y_{46} \end{bmatrix} \end{array} \begin{bmatrix} V_1 \\ V_2 \\ V_5 \\ V_6 \end{bmatrix}. \qquad (13)$$

From the rows ③ and ④,

$$\left.\begin{aligned} V_5&=(y_{33}V_1-y_{34}V_2)/y_{35} \\ V_6&=(-y_{34}V_1+y_{44}V_2)/y_{46}. \end{aligned}\right\} \qquad (14)$$

Substituting eq.(14) into the rows ① and ② in eq.(13), the final 2×2 admittance matrix representation is obtained as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad (15)$$

where

$$\left.\begin{aligned} Y_{11} &\triangleq y_{11}-y_{15}y_{33}/y_{35}=y_{10}+y_{12}-y_{15}(y_{30}+y_{34})/y_{35} \\ Y_{12} &\triangleq -y_{12}+y_{15}y_{34}/y_{35} \\ Y_{21} &\triangleq -y_{12}+y_{26}y_{34}/y_{46} \\ Y_{22} &\triangleq y_{22}-y_{26}y_{44}/y_{46}=y_{20}+y_{12}-y_{26}(y_{40}+y_{34})/y_{46}. \end{aligned}\right\} \qquad (16)$$

Matrix elements $Y_{11}-Y_{22}$ can take arbitrary values independently, because they have plus- and minus-terms and many freedoms.

The nullator-norator circuit for eq.(15) is shown in Fig. 5. This is the circuit proposed by Imai et al., but they derived it by NIC (Negative Impedance Converter) concept [7].

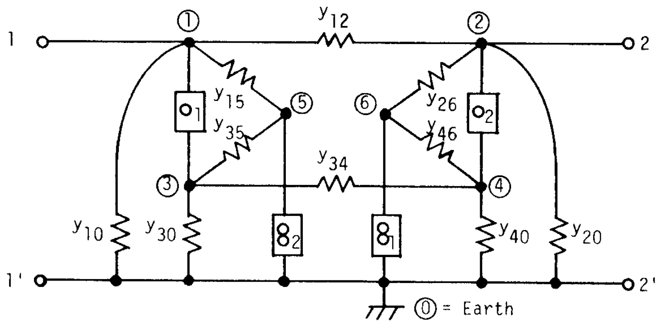


Fig. 5. TYPE II circuit for the realization of arbitrary 2×2 conductance matrix.

2.3 Derivation of TYPE III Circuit (New proposed circuit)

Another new circuit for the realization of arbitrary 2×2 conductance matrix can be derived by choosing another new set of admittance values in step 3 in Yanagisawa et al's original method.

(Step 3″) Choosing the admittances

$$y_{12}=y_{16}=y_{25}=y_{34}=y_{36}=y_{45}=0 \qquad (17)$$

in eq.(6) without loss of generality, the following expression is obtained

$$\begin{array}{cc} & \begin{array}{cccc} ①=③ & ②=④ & ⑤ & ⑥ \end{array} \\ \begin{array}{c} ① \\ ② \\ ③ \\ ④ \end{array} \begin{bmatrix} I_1 \\ I_2 \\ 0 \\ 0 \end{bmatrix} = & \begin{bmatrix} y_{11} & -y_{14} & -y_{15} & 0 \\ -y_{23} & y_{22} & 0 & -y_{26} \\ y_{33} & -y_{23} & -y_{35} & 0 \\ -y_{14} & y_{44} & 0 & -y_{46} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_5 \\ V_6 \end{bmatrix}. \end{array} \qquad (18)$$

From the rows ③ and ④,

$$\left.\begin{aligned} V_5&=(y_{33}V_1-y_{23}V_2)/y_{35} \\ V_6&=(-y_{14}V_1+y_{44}V_2)/y_{46}. \end{aligned}\right\} \qquad (19)$$

Substituting eq.(19) into the rows ① and ② in eq.(18), the final 2×2 admittance matrix representation is obtained as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad (20)$$

where

$$\left.\begin{aligned} Y_{11} &\triangleq y_{11}-y_{15}y_{33}/y_{35}=y_{10}+y_{14}-y_{15}(y_{30}+y_{23})/y_{35} \\ Y_{12} &\triangleq -y_{14}+y_{15}y_{23}/y_{35} \\ Y_{21} &\triangleq -y_{23}+y_{26}y_{14}/y_{46} \\ Y_{22} &\triangleq y_{22}-y_{26}y_{44}/y_{46}=y_{20}+y_{23}-y_{26}(y_{40}+y_{14})/y_{46}. \end{aligned}\right\} \qquad (21)$$

Matrix elements $Y_{11}-Y_{22}$ can take arbitrary values independently, because they have plus- and minus-terms and many freedoms.

The nullator-norator circuit for eq.(20) is shown in Fig. 6. This is a new proposed circuit.

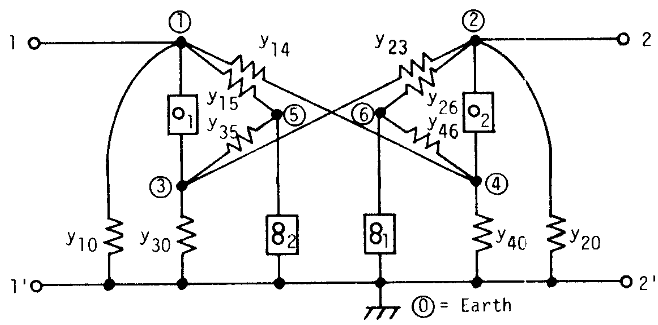


Fig. 6. TYPE III circuit for the realization of arbitrary 2×2 conductance matrix.

3. Applications to Impedance-matched Bilateral Amplifiers

In this section, the circuits of TYPE I, TYPE II, TYPE III shown in Figs. 4-6 are applied to the design of the impedance-matched bilateral amplifier using operational amplifiers and resistors. Their experimental results are also shown. Stability is checked by using the return difference matrix [8]-[11].

3.1 Principle of the Impedance-matched Bilateral Amplifier

The impedance-matched bilateral amplifier was proposed for the use in long-distance telephone transmission system [12].

This amplifier can amplify the signal from Port 1 (①-①') to Port 2 (②-②'), and also from Port 2 to Port 1 (Fig. 7). The input-impedances are matched at Port 1 and Port 2, therefore, the reflection of the signal does not occure.

In Fig. 7, the matching-admittances are given by

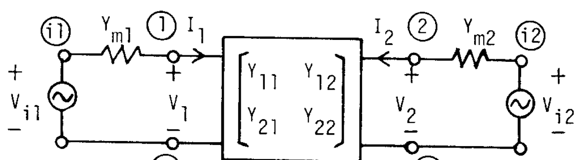
$$\left.\begin{aligned} Y_{m1} &\triangleq \sqrt{(Y_{11}/Y_{22})\cdot\triangle \mathbf{Y}} = G_1 \\ Y_{m2} &\triangleq \sqrt{(Y_{22}/Y_{11})\cdot\triangle \mathbf{Y}} = G_2 \end{aligned}\right\} \quad (22)$$

where

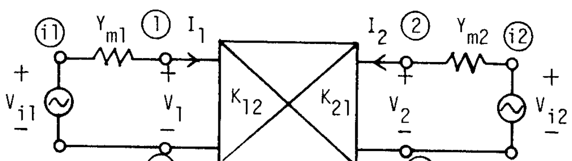
$$\triangle \mathbf{Y} \triangleq Y_{11}Y_{22} - Y_{12}Y_{21} = G_1G_2, \qquad (23)$$

and the transfer voltage gains are defined as

$$\left.\begin{aligned} K_{12} &\triangleq \frac{V_2}{V_1}\bigg|_{V_{i2}=0} = \frac{-Y_{21}}{Y_{22}+Y_{m2}} \quad (V_{i1}\text{: excited, } V_{i2}\text{: short-circuited})^{*} \\ K_{21} &\triangleq \frac{V_1}{V_2}\bigg|_{V_{i1}=0} = \frac{-Y_{12}}{Y_{11}+Y_{m1}} \quad (V_{i2}\text{: excited, } V_{i1}\text{: short-circuited})^{**}. \end{aligned}\right\} \quad (24)$$



(a) Impedance-matched two-port network.



(b) Impedance-matched bilateral amplifier.

Fig. 7. Two-port network and bilateral amplifier with matching-admittances Y_{m1} and Y_{m2}.

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*This operation is called "the K_{12} operation". **This operation is called "the K_{21} operation".

From eqs.(22)-(24), the conductance matrix is evaluated as

$$\mathbf{Y}=\begin{bmatrix} -(K_{12}K_{21}+1)G_1/(K_{12}K_{21}-1) & 2K_{21}G_1/(K_{12}K_{21}-1) \\ 2K_{12}G_2/(K_{12}K_{21}-1) & -(K_{12}K_{21}+1)G_2/(K_{12}K_{21}-1) \end{bmatrix}. \qquad (25)$$

This conductance matrix can be calculated from the given K_{12} and K_{21}, except for the case of $K_{12}K_{21}=1$. In technology, it is reasonable to be $|K_{12}|, |K_{21}|>1$, because the active elements, i.e. operational amplifiers, are used.

3.2 Design of Impedance-matched Bilateral Amplifier

As examples, the impedance-matched bilateral amplifiers with the gains $|K_{12}|=2$ (=6 dB), $|K_{21}|=4$ (=12 dB) and the matching-admittances $G \triangleq G_1=G_2=1/600$ S, are designed. From eq.(25), the conductance matrices are calculated as follows:

[Case A] $K_{12}=2$, $K_{21}=4$

$$\mathbf{Y}=\begin{bmatrix} -9G/7 & 8G/7 \\ 4G/7 & -9G/7 \end{bmatrix} \qquad (26)$$

[Case B] $K_{12}=2$, $K_{21}=-4$

$$\mathbf{Y}=\begin{bmatrix} -7G/9 & 8G/9 \\ -4G/9 & -7G/9 \end{bmatrix} \qquad (27)$$

[Case C] $K_{12}=-2$, $K_{21}=4$

$$\mathbf{Y}=\begin{bmatrix} -7G/9 & -8G/9 \\ 4G/9 & -7G/9 \end{bmatrix} \qquad (28)$$

[Case D] $K_{12}=-2$, $K_{21}=-4$

$$\mathbf{Y}=\begin{bmatrix} -9G/7 & -8G/7 \\ -4G/7 & -9G/7 \end{bmatrix} \qquad (29)$$

The bilateral amplifiers using TYPE I circuit shown in Fig. 4, TYPE II circuit shown in Fig. 5 and TYPE III circuit shown in Fig. 6 are realized by equating eqs.(26)-(29) to eqs.(10), (15) and (20), respectively. As an example, the design procedure for the realization circuit of case A using TYPE III circuit (Fig. 6) is illustrated:

[TYPE III-Case A] The admittance values can be determined as follows.

(Step 1) From eqs.(20) and (26), choose

$$y_{10}=y_{20}=0. \qquad (30)$$

Then

$$Y_{11}=y_{14}-y_{15}(y_{30}+y_{23})/y_{35}=-9G/7 \qquad (31)$$

$$Y_{12}=-y_{14}+y_{15}y_{23}/y_{35}=8G/7 \qquad (32)$$

$$Y_{21}=-y_{23}+y_{26}y_{14}/y_{46}=4G/7 \qquad (33)$$

$$Y_{22}=y_{23}-y_{26}(y_{40}+y_{14})/y_{46}=-9G/7. \qquad (34)$$

(Step 2) From eqs.(31) and (32),

$$Y_{11}+Y_{12}=-y_{15}y_{30}/y_{35}=-G/7. \qquad (35)$$

Choose

$$y_{15}=10y_{35}=G/2=1/1200\,\mathrm{S}. \qquad (36)$$

Then

$$y_{30}=G/70=1/42000\,\mathrm{S}. \qquad (37)$$

(Step 3) From eqs.(33) and (34),

$$Y_{21}+Y_{22}=-y_{26}y_{40}/y_{46}=-5G/7. \qquad (38)$$

Choose

$$y_{26}=10y_{46}=2G/5=1/1500\,\mathrm{S}. \qquad (39)$$

Then

$$y_{40}=5G/70=1/8400\,\mathrm{S}. \qquad (40)$$

(Step 4) From eqs.(32), (33), (36) and (39),

$$Y_{12}+10Y_{21}=99y_{14}=48G/7. \qquad (41)$$

Therefore

$$y_{14}=16G/231=1/8662.5\,\mathrm{S}. \qquad (42)$$

(Step 5) From eqs.(33), (39) and (42),

$$y_{23}=10y_{14}-4G/7=4G/33=1/4950\,\mathrm{S}. \qquad (43)$$

This realization circuit is shown in Fig. 10 (a).

Similarly, the admittance values of another realization circuits can be determined, as shown in Figs. 8-10. These admittance values are determined so that the maximum output power of operational amplifiers is about 50 mW.

3.3 Stability of the Circuits Realized with Operational Amplifiers

In replacing nullators and norators to the actual operational amplifiers, the stability problem, which includes (1) the selection of nullator-norator pairs and (2) the determination of the input polarities of operational amplifiers, must be investigated [9]-[11],[13]. Stability can be checked by using the return difference matrix [8]-[11] for the associated VCVS circuit, where VCVS (Voltage-Controlled Voltage-Source) is taken as a macro-model of operational amplifier. In Figs. 8-10, the i-th nullator and the i-th norator form the i-th operational amplifier ($i=1, 2$), and the signs + and − at nullators indicate the input polarities of operational amplifiers, as shown in Fig. 1.

As an example, stability of the circuit of TYPE III-Case A shown in Fig. 10 (a) is analyzed:

[TYPE III-Case A] The transfer matrix $-\mathbf{H}_{32}$, in which the (i,j) element represents the voltage transfer ratio from the output of the j-th operational amplifier to the input of the i-th operational amplifier [9]-[11], is evaluated as

$$-\mathbf{H}_{32}=\begin{bmatrix} 0.156873 & -0.038488 \\ -0.027202 & 0.128339 \end{bmatrix}. \tag{44}$$

Hence, the return difference matrix $\mathbf{F}_d$ is evaluated as

$$\mathbf{F}_d \triangleq \mathbf{1}-\mathbf{KH}_{32} \tag{45}$$

$$=\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}+\begin{bmatrix} \mu_1 & 0 \\ 0 & \mu_2 \end{bmatrix}\begin{bmatrix} 0.156873 & -0.038488 \\ -0.027202 & 0.128339 \end{bmatrix} \tag{46}$$

$$=\begin{bmatrix} 1+0.156873\mu_1 & -0.038488\mu_1 \\ -0.027202\mu_2 & 1+0.128339\mu_2 \end{bmatrix} \tag{47}$$

where μ_1 and μ_2 denote the voltage gains of operational amplifiers 1 and 2 respectively. The determinant of this matrix is calculated as

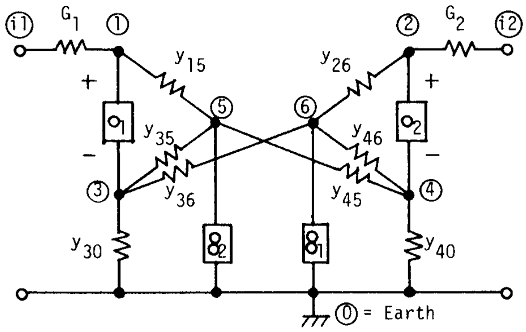
$$\det \mathbf{F}_d = 1+0.156873\mu_1+0.128339\mu_2+0.01908597\mu_1\mu_2. \tag{48}$$

In this expression, all coefficients for μ_1, μ_2 and $\mu_1\mu_2$ are positive, therefore, this circuit is "absolutely DC stable" [9]-[11], [13].

Similarly, another circuits shown in Figs. 8-10 are all "absolutely DC stable".

[Remark] DC stability is a necessary condition for asymptotic stability [11]. However, if a circuit contains one or two active elements (e.g. operational amplifiers) and if the active elements possess the first-order phase-lag characteristics, DC stability becomes the necessary and sufficient condition for it [10]. The 741 type operational amplifiers (e.g. MC1741CG) can be assumed to possess the above characteristics [14], [15]. Therefore, all realized circuits of Figs. 8-10 are always stable in any activation, because two operational amplifiers MC1741CG are used. This is confirmed by the experiments, as shown in the following subsection 3. 4.

TYPE I-Case A circuit shown in Fig. 8(a) corresponds to Yanagisawa et al's circuit [2], and TYPE I-Case D circuit shown in Fig. 8(d) corresponds to Kambayashi's circuit [3], and TYPE II-Case A circuit shown in Fig. 9(a) corresponds to Imai et al's circuit [4], [7]. Another circuits in Figs. 8-10 are new circuit configurations for the realization of impedance-matched bilateral amplifier.



Designated values:

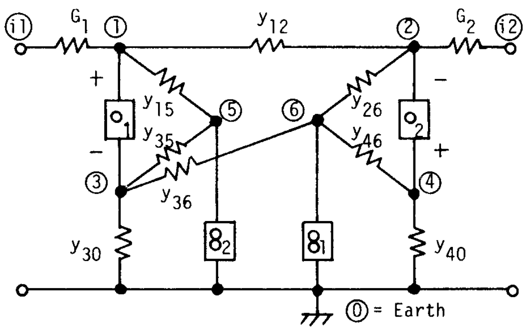
$G_1 = G_2 = G$ (600Ω)
$y_{12} = y_{16} = y_{25} = 0$
$y_{11} = y_{15} = y_{22} = y_{26} = G$ (600Ω)
$y_{33} = y_{44} = 3G/10$ (2kΩ)

Evaluated values:

$y_{10} = y_{20} = 0$
$y_{35} = y_{46} = 3G/20$ (4kΩ)
$y_{36} = y_{30} = 3G/40$ (8kΩ)
$y_{45} = 3G/80$ (16kΩ)
$y_{40} = 9G/80$ (5.3333kΩ)

$$-H_{32} = \begin{bmatrix} 0.272727 & 0.000000 \\ 0.055556 & 0.125683 \end{bmatrix}$$

(a) TYPE I - Case A ($K_{12} = 2$, $K_{21} = 4$)



Designated values:

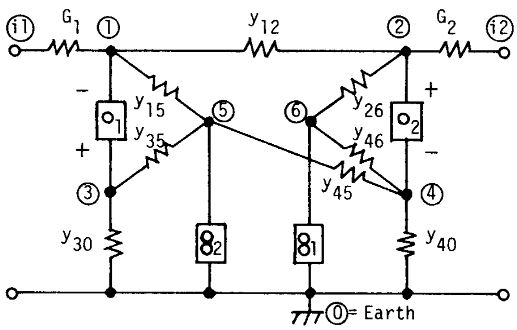
$G_1 = G_2 = G$ (600Ω)
$y_{10} = y_{20} = y_{16} = y_{25} = y_{45} = 0$
$y_{26} = 5y_{46} = 3G/10$ (2kΩ)
$y_{15} = 5y_{35} = 3G/10$ (2kΩ)

Evaluated values:

$y_{12} = 4G/9$ (1.35kΩ)
$y_{40} = 11G/45$ (2.4545kΩ)
$y_{36} = 36G/685$ (11.417kΩ)
$y_{30} = 1183G/6165$ (3.1268kΩ)

$$-H_{32} = \begin{bmatrix} 0.172113 & 0.016327 \\ -0.013114 & 0.049641 \end{bmatrix}$$

(b) TYPE I - Case B ($K_{12} = 2$, $K_{21} = -4$)



Designated values:

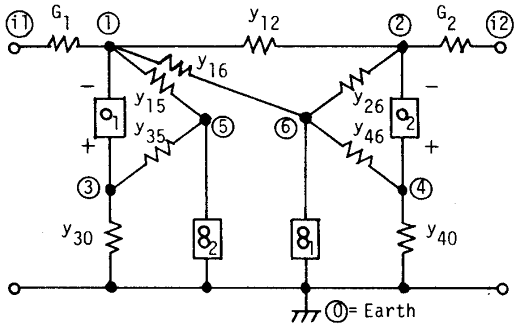
$G_1 = G_2 = G$ (600Ω)
$y_{10} = y_{20} = y_{16} = y_{25} = y_{36} = 0$
$y_{15} = 5y_{35} = 3G/10$ (2kΩ)
$y_{26} = 5y_{46} = 3G/10$ (2kΩ)

Evaluated values:

$y_{12} = 8G/9$ (675Ω)
$y_{30} = G/3$ (1.8kΩ)
$y_{40} = 259G/885$ (2.0502kΩ)
$y_{45} = 12G/295$ (14.75kΩ)

$$-H_{32} = \begin{bmatrix} 0.070922 & 0.014124 \\ -0.017007 & 0.038169 \end{bmatrix}$$

(c) TYPE I - Case C ($K_{12} = -2$, $K_{21} = 4$)



Designated values:

$G_1 = G_2 = G$ (600Ω)
$y_{10} = y_{20} = y_{25} = y_{36} = y_{45} = 0$
$y_{26} = 5y_{46} = 3G/10$ (2kΩ)
$y_{15} = 5y_{35} = 3G/10$ (2kΩ)

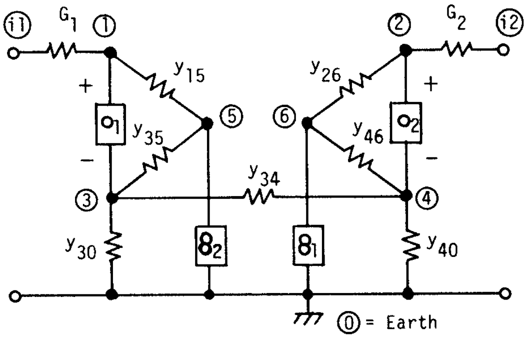
Evaluated values:

$y_{12} = 4G/7$ (1.05kΩ)
$y_{40} = 13G/35$ (1.6154kΩ)
$y_{16} = 12G/151$ (7.55kΩ)
$y_{30} = 2047G/5285$ (1.5491kΩ)

$$-H_{32} = \begin{bmatrix} 0.050314 & 0.036232 \\ 0.028736 & 0.055556 \end{bmatrix}$$

(d) TYPE I - Case D ($K_{12} = -2$, $K_{21} = -4$)

Fig. 8. TYPE I circuits of the impedance-matched bilateral amplifiers.



Designated values:

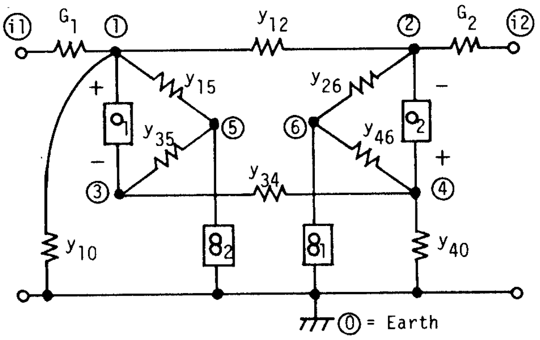
$$\begin{cases} G_1 = G_2 = G \ (600\Omega) \\ y_{10} = y_{20} = y_{12} = 0 \\ y_{35} = y_{46} = 0.5y_{34} = 3G/50 \ (10\mathrm{k}\Omega) \end{cases}$$

Evaluated values:

$$\begin{cases} y_{15} = 4G/7 \ (1.05\mathrm{k}\Omega) \\ y_{26} = 2G/7 \ (2.1\mathrm{k}\Omega) \\ y_{30} = 3G/200 \ (40\mathrm{k}\Omega) \\ y_{40} = 3G/20 \ (4\mathrm{k}\Omega) \end{cases}$$

$$-H_{32} = \begin{bmatrix} 0.142012 & 0.048128 \\ 0.008547 & 0.154412 \end{bmatrix}$$

(a) TYPE II - Case A ($K_{12} = 2$, $K_{21} = 4$)



Designated values:

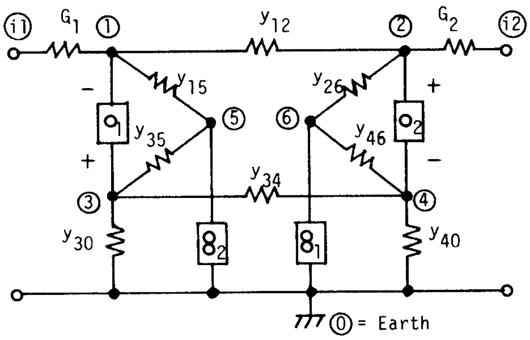
$$\begin{cases} G_1 = G_2 = G \ (600\Omega) \\ y_{20} = y_{30} = 0 \\ y_{26} = 2y_{46} = 3G/11 \ (2.2\mathrm{k}\Omega) \\ y_{12} = 2G/3 \ (900\Omega) \\ y_{15} = 6G/13 \ (1.3\mathrm{k}\Omega) \end{cases}$$

Evaluated values:

$$\begin{cases} y_{10} = y_{34} = G/9 \ (5.4\mathrm{k}\Omega) \\ y_{40} = 11G/18 \ (981.82\Omega) \\ y_{35} = 3G/91 \ (18.2\mathrm{k}\Omega) \end{cases}$$

$$-H_{32} = \begin{bmatrix} 0.070309 & 0.018804 \\ 0.000000 & 0.047734 \end{bmatrix}$$

(b) TYPE II - Case B ($K_{12} = 2$, $K_{21} = -4$)



Designated values:

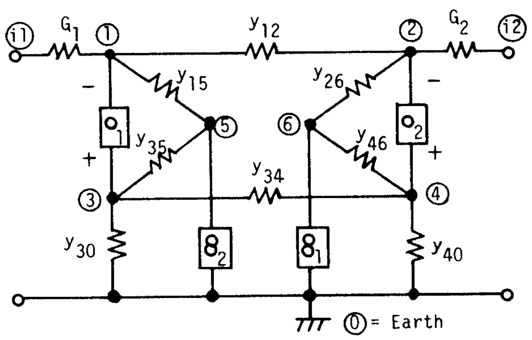
$$\begin{cases} G_1 = G_2 = G \ (600\Omega) \\ y_{10} = y_{20} = 0 \\ y_{15} = 3y_{35} = 3G/11 \ (2.2\mathrm{k}\Omega) \\ y_{12} = G \ (600\Omega) \\ y_{26} = 2G/5 \ (1.5\mathrm{k}\Omega) \end{cases}$$

Evaluated values:

$$\begin{cases} y_{30} = 5G/9 \ (1.08\mathrm{k}\Omega) \\ y_{34} = G/27 \ (16.2\mathrm{k}\Omega) \\ y_{46} = 6G/585 \ (58.5\mathrm{k}\Omega) \\ y_{40} = G/117 \ (70.2\mathrm{k}\Omega) \end{cases}$$

$$-H_{32} = \begin{bmatrix} 0.085098 & 0.028018 \\ 0.014639 & 0.013607 \end{bmatrix}$$

(c) TYPE II - Case C ($K_{12} = -2$, $K_{21} = 4$)



Designated values:

$$\begin{cases} G_1 = G_2 = G \ (600\Omega) \\ y_{10} = y_{20} = 0 \\ y_{12} = 3G/2 \ (400\Omega) \\ y_{15} = 2y_{35} = 3G/10 \ (2\mathrm{k}\Omega) \\ y_{26} = 3G/10 \ (2\mathrm{k}\Omega) \end{cases}$$

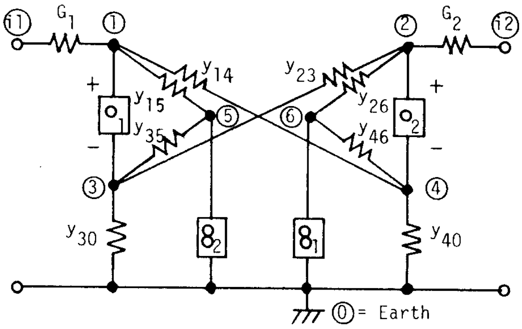
Evaluated values:

$$\begin{cases} y_{34} = 5G/28 \ (3.36\mathrm{k}\Omega) \\ y_{30} = 17G/14 \ (494.12\Omega) \\ y_{46} = 3G/52 \ (10.4\mathrm{k}\Omega) \\ y_{40} = 5G/14 \ (1.68\mathrm{k}\Omega) \end{cases}$$

$$-H_{32} = \begin{bmatrix} 0.079330 & 0.065543 \\ 0.063218 & 0.061636 \end{bmatrix}$$

(d) TYPE II - Case D ($K_{12} = -2$, $K_{21} = -4$)

Fig. 9. TYPE II circuits of the impedance-matched bilateral amplifiers.



Designated values:

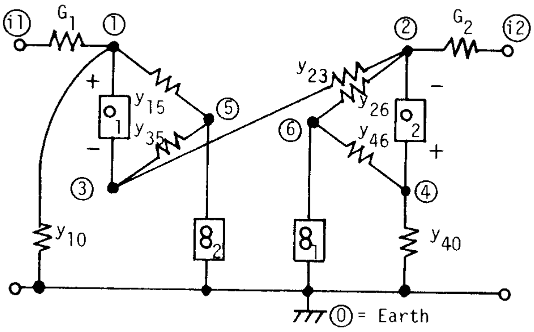
$$\begin{cases} G_1 = G_2 = G \ (600\Omega) \\ y_{10} = y_{20} = 0 \\ y_{15} = 10y_{35} = G/2 \ (1.2\mathrm{k}\Omega) \\ y_{26} = 10y_{46} = 2G/5 \ (1.5\mathrm{k}\Omega) \end{cases}$$

Evaluated values:

$$\begin{cases} y_{30} = G/70 \ (42\mathrm{k}\Omega) \\ y_{40} = 5G/70 \ (8.4\mathrm{k}\Omega) \\ y_{14} = 16G/231 \ (8.6625\mathrm{k}\Omega) \\ y_{23} = 4G/33 \ (4.95\mathrm{k}\Omega) \end{cases}$$

$$-H_{32} = \begin{bmatrix} 0.156873 & -0.038488 \\ -0.027202 & 0.128339 \end{bmatrix}$$

(a) TYPE Ⅲ - Case A $(K_{12} = 2,\ K_{21} = 4)$



Designated values:

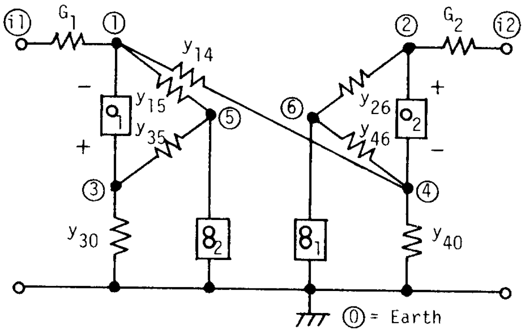
$$\begin{cases} G_1 = G_2 = G \ (600\Omega) \\ y_{20} = y_{30} = y_{14} = 0 \\ y_{15} = 3G/10 \ (2\mathrm{k}\Omega) \\ y_{26} = 5y_{46} = 3G/10 \ (2\mathrm{k}\Omega) \end{cases}$$

Evaluated values:

$$\begin{cases} y_{23} = 4G/9 \ (1.35\mathrm{k}\Omega) \\ y_{10} = G/9 \ (5.4\mathrm{k}\Omega) \\ y_{35} = 3G/20 \ (4\mathrm{k}\Omega) \\ y_{40} = 11G/45 \ (2.4545\mathrm{k}\Omega) \end{cases}$$

$$-H_{32} = \begin{bmatrix} 0.149533 & 0.103641 \\ 0.006452 & 0.085470 \end{bmatrix}$$

(b) TYPE Ⅲ - Case B $(K_{12} = 2,\ K_{21} = -4)$



Designated values:

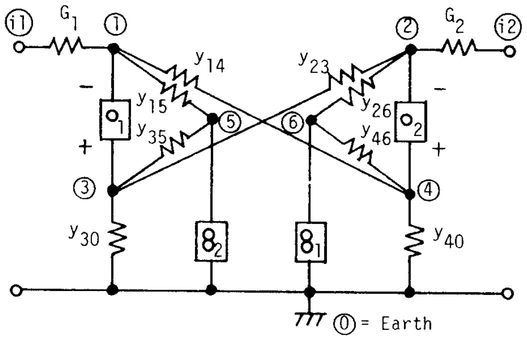
$$\begin{cases} G_1 = G_2 = G \ (600\Omega) \\ y_{10} = y_{20} = y_{23} = 0 \\ y_{26} = 3G/25 \ (5\mathrm{k}\Omega) \\ y_{15} = 5y_{35} = 3G/10 \ (2\mathrm{k}\Omega) \end{cases}$$

Evaluated values:

$$\begin{cases} y_{14} = 8G/9 \ (675\Omega) \\ y_{46} = 6G/25 \ (2.5\mathrm{k}\Omega) \\ y_{40} = 2G/3 \ (900\Omega) \\ y_{30} = G/3 \ (1.8\mathrm{k}\Omega) \end{cases}$$

$$-H_{32} = \begin{bmatrix} 0.088710 & 0.017582 \\ 0.086406 & 0.084171 \end{bmatrix}$$

(c) TYPE Ⅲ - Case C $(K_{12} = -2,\ K_{21} = 4)$



Designated values:

$$\begin{cases} G_1 = G_2 = G \ (600\Omega) \\ y_{10} = y_{20} = 0 \\ y_{14} = 3G/2 \ (400\Omega) \\ y_{23} = 3G/4 \ (800\Omega) \\ y_{15} = G/7 \ (4.2\mathrm{k}\Omega) \\ y_{26} = G/14 \ (8.4\mathrm{k}\Omega) \end{cases}$$

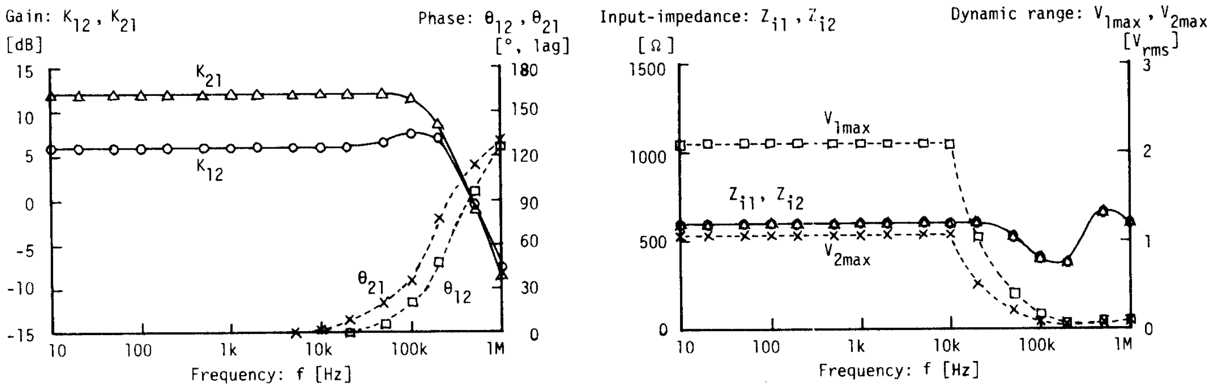
Evaluated values:

$$\begin{cases} y_{35} = 3G/10 \ (2\mathrm{k}\Omega) \\ y_{30} = 51G/10 \ (117.65\Omega) \\ y_{46} = 3G/5 \ (1\mathrm{k}\Omega) \\ y_{40} = 78G/5 \ (38.462\Omega) \end{cases}$$

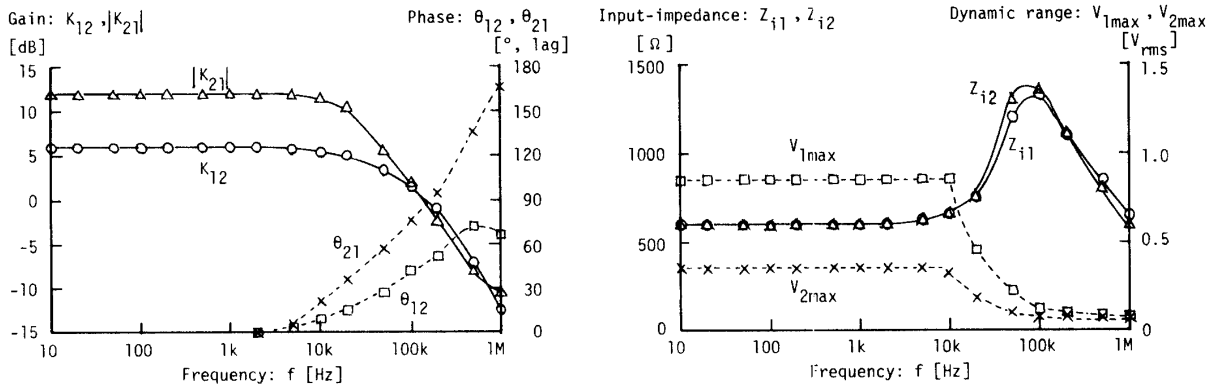
$$-H_{32} = \begin{bmatrix} 0.013736 & 0.008561 \\ 0.011638 & 0.013795 \end{bmatrix}$$

(d) TYPE Ⅲ - Case D $(K_{12} = -2,\ K_{21} = -4)$

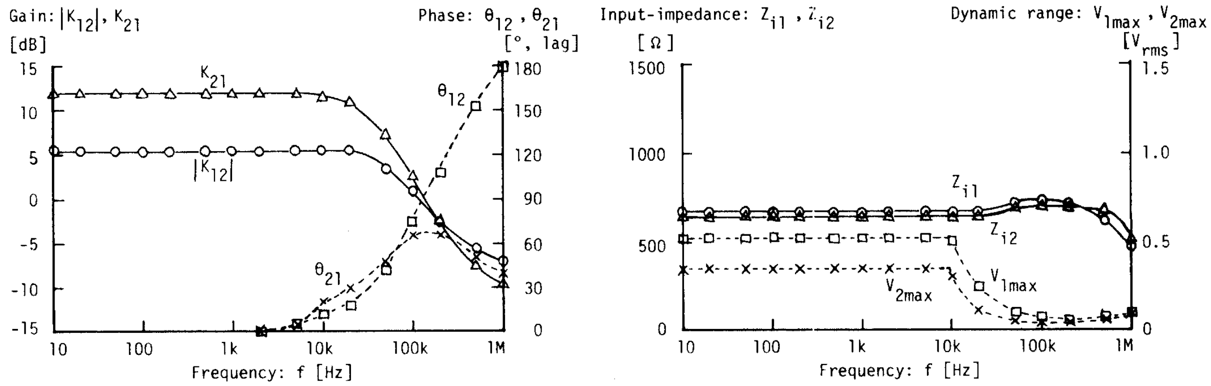
Fig. 10. TYPE Ⅲ circuits of the impedance-matched bilateral amplifiers.



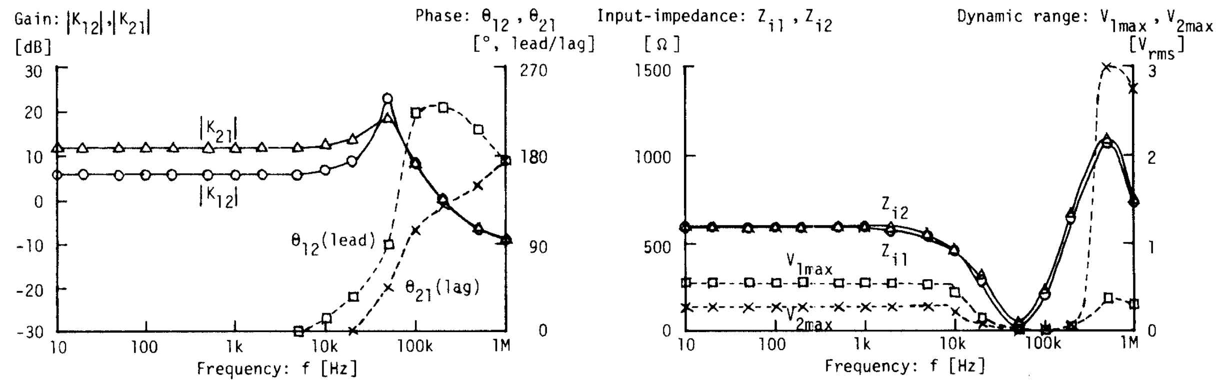
(a) TYPE I - Case A ($K_{12}=2$, $K_{21}=4$)



(b) TYPE I - Case B ($K_{12}=2$, $K_{21}=-4$)

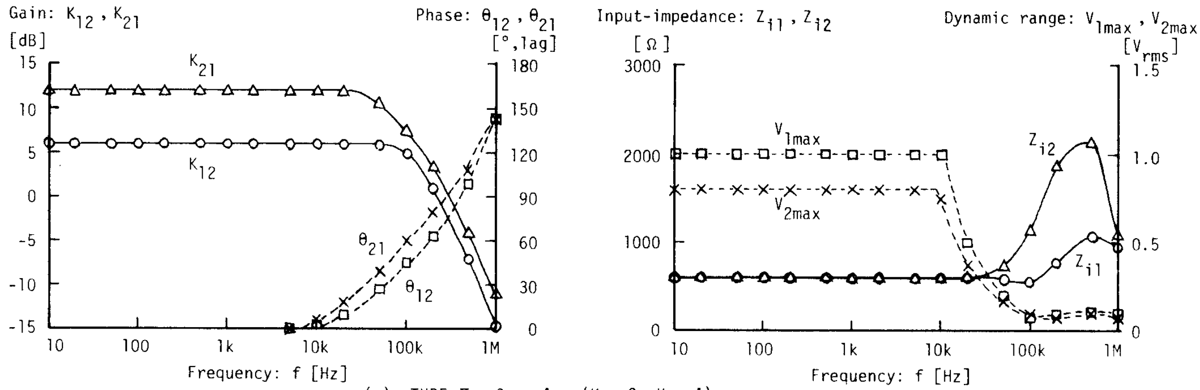


(c) TYPE I - Case C ($K_{12}=-2$, $K_{21}=4$)

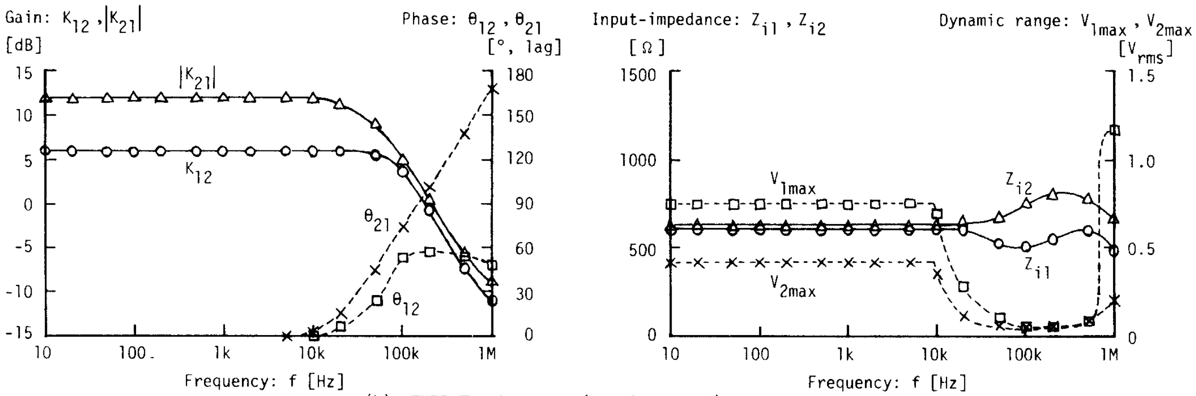


(d) TYPE I - Case D ($K_{12}=-2$, $K_{21}=-4$)

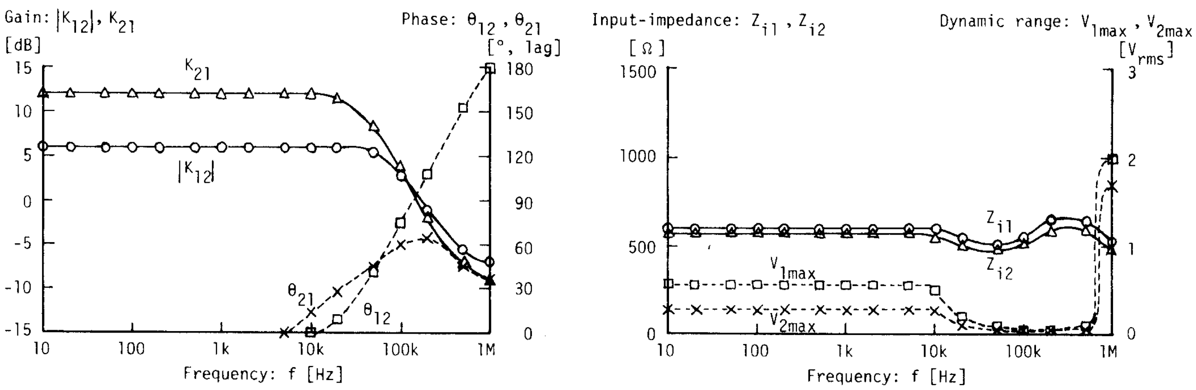
Fig. 11. Measured frequency characteristics for TYPE I circuits of the impedance-matched bilateral amplifiers shown in Fig. 8 (Temperature: Ta = 15°C).



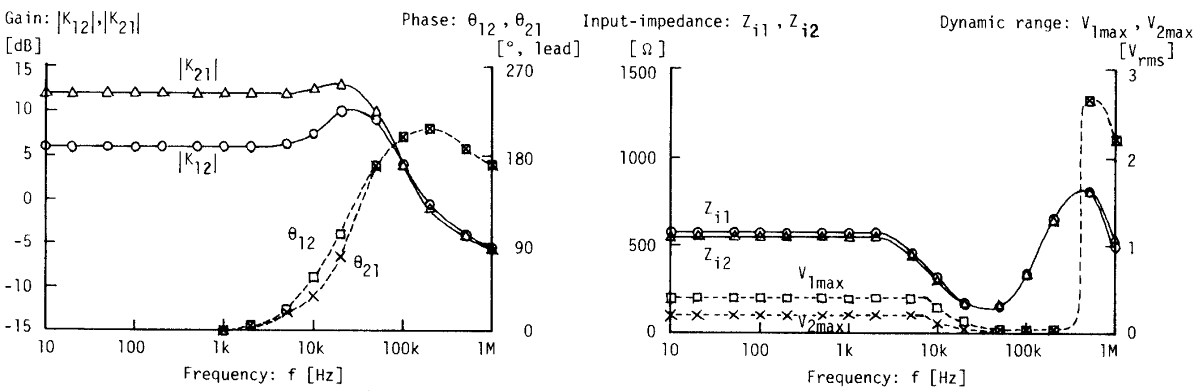
(a) TYPE II - Case A (K_{12}=2, K_{21}=4)



(b) TYPE II - Case B (K_{12}=2, K_{21}=-4)

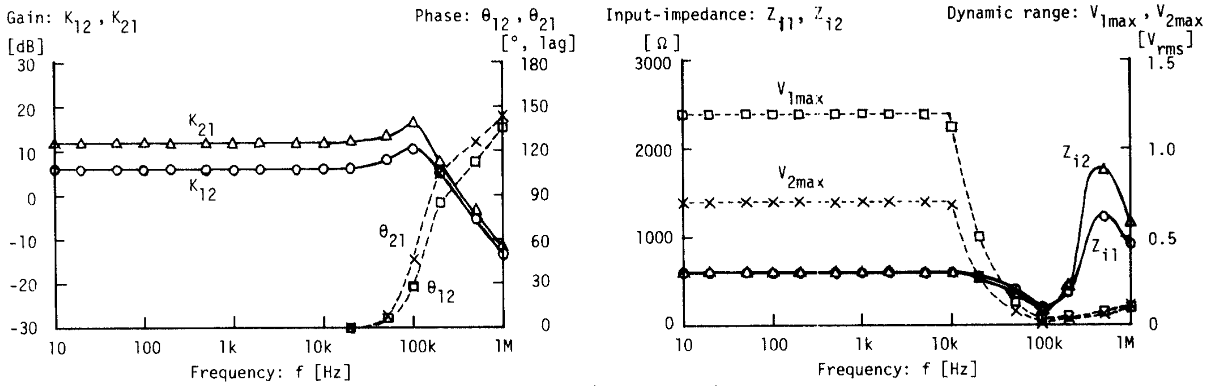


(c) TYPE II - Case C (K_{12}=-2, K_{21}=4)

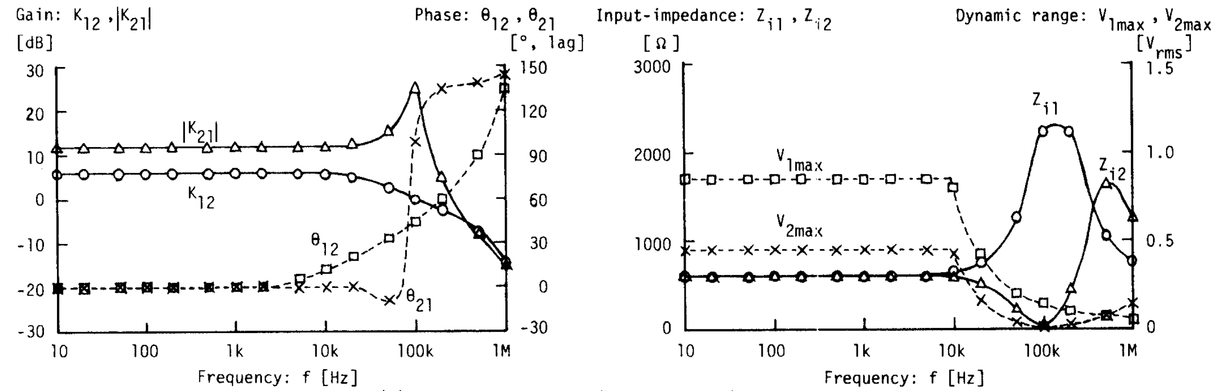


(d) TYPE II - Case D (K_{12}=-2, K_{21}=-4)

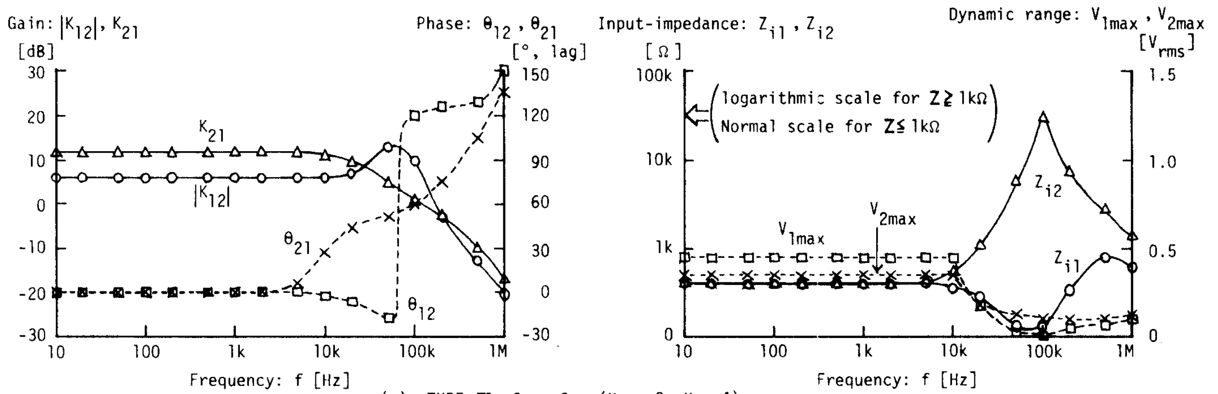
Fig. 12. Measured frequency characteristics for TYPE II circuits of the impedance-matched bilateral amplifiers shown in Fig. 9 (Temperature: Ta = 15°C).



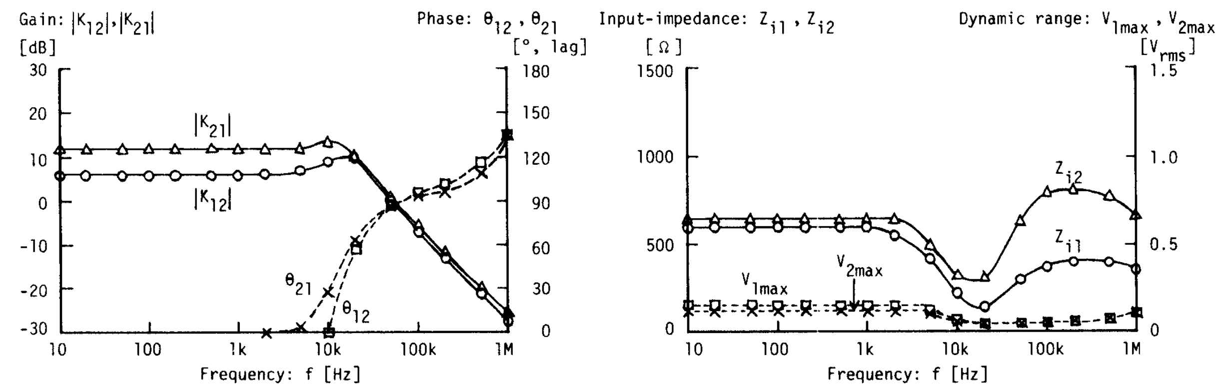
(a) TYPE Ⅲ - Case A ($K_{12}=2$, $K_{21}=4$)



(b) TYPE Ⅲ - Case B ($K_{12}=2$, $K_{21}=-4$)



(c) TYPE Ⅲ - Case C ($K_{12}=-2$, $K_{21}=4$)



(d) TYPE Ⅲ - Case D ($K_{12}=-2$, $K_{21}=-4$)

Fig. 13. Measured frequency characteristics for TYPE Ⅲ circuits of the impedance-matched bilateral amplifiers shown in Fig. 10 (Temperature: Ta=15°C).

3.4 Experimental Results

The impedance-matched bilateral amplifier circuits shown in Figs. 8-10 are implemented by using operational amplifiers MC1741CG (Motorola) with DC supply voltage $V_S = \pm 15\,V$. The used resistors are selected under 0.1 % error.

Their experimental results are shown in Figs. 11-13. The transfer voltage gains K_{12} and K_{21}, the phase lag (or lead) $\theta_{12} \triangleq \angle(V_2/V_1)$ and $\theta_{21} \triangleq \angle(V_1/V_2)$, the input impedances $Z_{i1} \triangleq |V_1/I_1| = |V_1/(V_{i1}-V_1)G_1|$ and $Z_{i2} \triangleq |V_2/I_2| = |V_2/(V_{i2}-V_2)G_2|$, and the dynamic ranges V_{1max} and V_{2max}, which is the maximum input voltages under 2 % output distortion, are measured in the K_{12} and K_{21} operations (see eq.(24)), respectively. The ideal characteristics are as follows: (1) $|K_{12}| = 6\,dB$ constant, and $|K_{21}| = 12\,dB$ constant; (2) $\theta_{12} = \theta_{21} = 0°$ constant; (3) $Z_{i1} = Z_{i2} = 600\,\Omega$ constant; (4) V_{1max} and V_{2max} are large. In the low-frequency range of $f \leqq 10$ kHz, the measured characteristics satisfy the ideal characteristics as shown in Figs. 11-13, i.e., these implemented bilateral amplifier circuits function as desired. However, in the high-frequency range of $f \geqq 10$ kHz, the measured characteristics deviate from the ideal characteristics, because the actual operational amplifiers have the phase-shift characteristics.

For the practical use, sensitivity, temperature characteristics, noise characteristics, etc. must be investigated, too. Table 1 shows the general evaluation for the practical use, including these investigations.

Table 1. General evaluation for the realized circuits shown in Figs. 8-10.
(◎: excellent, ○: good, △: poor)

Case \ TYPE	I	II	III
A	◎	◎	○
B	○	◎	○
C	○	○	△
D	○	○	△

4. Conclusion

Three types of circuits for the realization of arbitrary 2×2 conductance matrix using two nullators and two norators have been derived systematically by Yanagisawa et al's method. One of them is a new circuit which is shown in Fig. 6. They have been applied to the design of impedance-matched bilateral amplifiers with the gains $|K_{12}| = 2$ and $|K_{21}| = 4$ and the matching-impedances $G_1^{-1} = G_2^{-1} = 600\,\Omega$. These bilateral amplifiers have been implemented by using operational amplifiers and resistors. The measured data indicate that they function satisfactory in the low-frequency range of $f \leqq 10$ kHz.

Operational amplifiers are widely used in the electronic analog circuits because of their low cost and high performance. The nullator-norator concept is going to be employed more and more in the electronic circuit design.

Acknowledgement

The author would like to thank Prof. Dr. Tadashi Matsumoto of Fukui University for his helpful discussion and encouragement.

References

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