A Universal Nullor and Its Applications to The nct-α Type Two-Port Realization

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Abstract — An implementation of the universal nullor is proposed by using transistors, diodes, resistors and capacitors. It has both the input and output ports independently floating and is very usefull to the designer of accurate analog electronic systems in minimizing the required number of active elements and passive precision elements. It is applied to the nct-α type two-port realization, and the electrical insulation property between ports of two-port is examined.

1. Introduction

Active networks have been realized in the low frequency range by using the usual IC operational amplifiers having the grounded output port or the differential output port, because of their low cost and high performance [1]. The grounded output type IC operational amplifier is an implementation of an unbalanced nullor with the grounded norator. The differential output type IC operational amplifier is an implementation of a balanced nullor, but not a universal nullor. It can be used only in AC mode and has the following features: (1) The output port cannot be grounded in DC mode or in AC mode. (2) The DC potential of output port is fixed at a constant DC potential.

Recently, however, the unusual IC operational amplifier, which has both the input and output ports independently floating, was developed by Huijsing and Korte [2]. This operational amplifier corresponds to a balanced and universal nullor which can be used both in DC mode and in AC mode and can be also used both in the four-terminal configulation and in the three-terminal configulation in any networks.

In this paper, an implementation of the balanced and universal nullor, which is a modified version of Huijsing [2], is proposed. The difference of this circuit from the Huijsing's is that the level shift stage is not used in this paper because the input and output stages are complementarily cascaded. This implemented circuit is applied to the nct-α type two-port realization, where the nct-α type two-port is defined as the noncommon-terminal type

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two-port having a cutset of nullators and a cutset of norators between port 1 and port 2. The electrical insulation property between ports in the nct-α type two-port is examined.

2. Implementation of The Universal Nullor

A nullor is an abbreviation of a nullator-norator pair shown in Fig. 1 and has the port characteristics obeying the relations [3] :

$$v_1 \equiv 0, \quad i_1 \equiv 0,$$

$$v_2 = \text{arbitrary}, \quad i_2 = \text{arbitrary}.$$

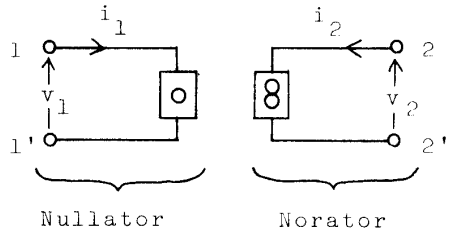


Fig. 1. Four-terminal nullor (or balanced nullor).

In this paper, a universal nullor is defined as a nullor with fully floating input and output ports.

2.1 The Basic Circuit Principle of The Universal Nullor

A universal nullor has the following two properties [2], [4] :

(1) It can be used both in the four-terminal configulation and in the three-terminal configuration.

(2) As the input and output ports of a universal nullor are independently floated from the ground, each terminal of a universal nullor can be independently connected to any point with arbitrary DC potential in the external network.

The implementations of typical nullors are shown in Fig. 2, where the signs, + and −, at the input and output ports mean the polarities. The basic circuit principles shown in Fig. 2 (a), (b), and (c) are extracted from their practical circuit diagrams [5], [6], and [2], respectively. Fig. 2 (d) shows our proposed basic circuit principle of a universal nullor [4].

The features of these implementations of typical nullors are as follows :

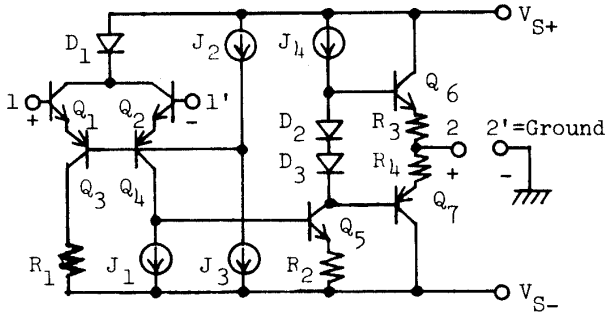
(a) A grounded output type IC operational amplifier (μA 741, Fairchild) :

It consists of a differential input stage (Q_1 to Q_4), a common-emitter stage (Q_5), and a class B push-pull output stage (Q_6, Q_7). The part of D_1 and Q_1 to Q_4 operates as a pnp type differential amplifier having good characteristics for practical use [7]. One of the output terminals is connected to the ground. Therefore, this circuit is the implementation of an unbalanced nullor, i. e., a nullor with the grounded norator.

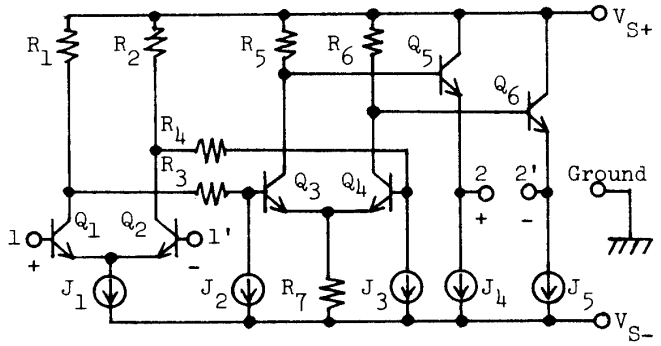
(b) A differential output type IC operational amplifier (MC 1520, Motorola) :

It consists of a differential input stage (Q_1, Q_2), a level shift stage (R_3, J_2 and R_4, J_3), a second differential amplifier stage (Q_3, Q_4), and a emitter follower output stage (Q_5, Q_6). The output port cannot be grounded in DC mode or in AC mode, and the DC potential of the output port is fixed at the ground potential. Therefore, this circuit is the implemen-

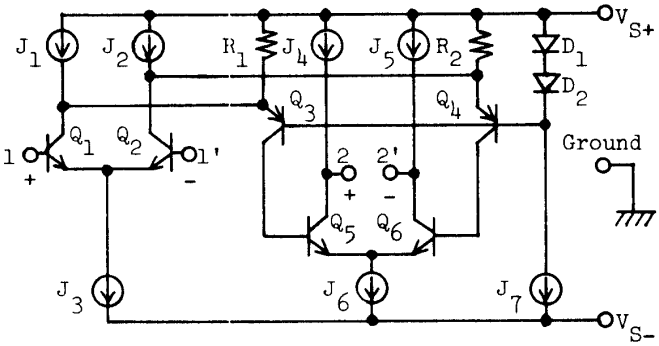
tation of a balanced nullor, but not a universal nullor.



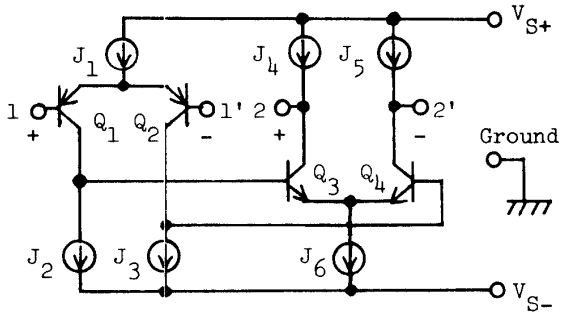
(a) A grounded output type IC operational amplifier (μA741, Fairchild), where $J_2 \simeq J_3$.



(b) A differential output type IC operational amplifier (MC1520, Motorola), where $J_2=J_3$, $J_4=J_5$, $R_1=R_2$, $R_3=R_4$ and $R_5=R_6$.



(c) A fully floating input and output type IC operational amplifier of Huijsing, where $J_3=2J_1=2J_2$, $J_6=2J_4=2J_5$ and $R_1=R_2$.



(d) Our proposed basic circuit principle of a balanced and universal nullor, where $J_1=2J_2=2J_3$ and $J_6=2J_4=2J_5$.

Fig. 2. The basic circuit principles of implementations of typical nullors.

(c) A fully floating input and output type IC operational amplifier of Huijsing [2] :

This basic circuit principle corresponds to the implementation of a balanced and universal nullor. It consists of a differential input stage (Q_1, Q_2), a level shift stage (Q_3, Q_4), and a differential output stage (Q_5, Q_6). As the input and output transistors are only npn types, the level shift stage is needed between the input and output stages. The input stage is floated by using three constant current sources J_1, J_2 and J_3, and the output stage is floated by using three constant current sources J_4, J_5 and J_6. The arbitrariness of the potential difference between the input and output stages is satisfied by the complementary cascade connection of the level shift stage and the output stage.

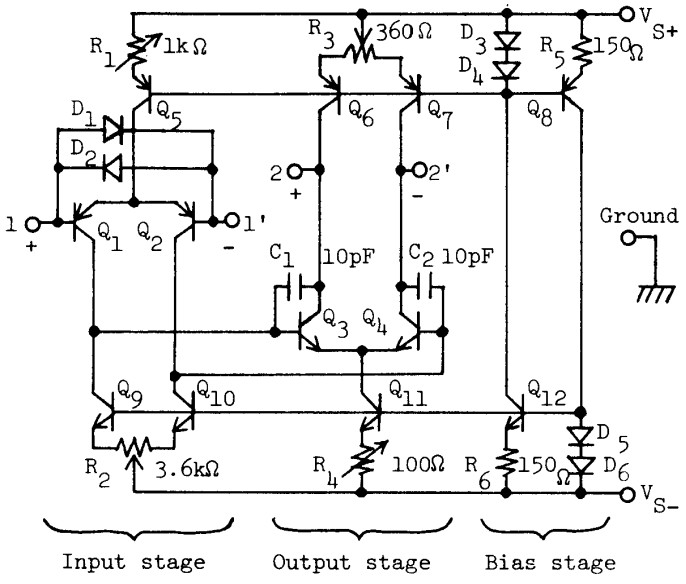
(d) Our proposed basic circuit principle of a balanced and universal nullor :

This is a modified version of the monolithic nullor of Huijsing [2]. It consists of a differential input stage (Q_1, Q_2) and a differential output stage (Q_3, Q_4). The level shift stage is not needed, because the input stage and the output stage are complementarily cascaded. The floating property of the input stage is satisfied by using three constant current sources

J_1, J_2 and J_3, and that of the output stage is satisfied by using three constant current sources J_4, J_5 and J_6. The arbitrariness of the potential difference between the input and output stages is satisfied by their complementary cascade connection, and the degree of the electrical insulation between them depends on the idealities of the transistors Q_1 to Q_4, i. e., the magnitudes of the collector resistances.

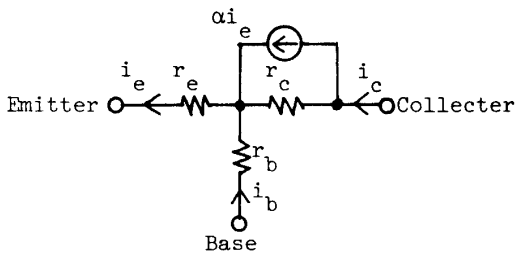
A breaf explanation for the operation principle of the nullor shown in Fig. 2 (d) is as follows: If the current flowing into the terminal 1 is increased by Δi_1 [A], then (1) the collector current of Q_1 is decreased by $h_{FE1} \times \Delta i_1$ [A], (2) this quantity is transfered to the base of Q_3, (3) the collector current of Q_3 is decreased by $h_{FE3} \times h_{FE1} \times \Delta i_1$ [A], and (4) this quantity flows out from the terminal 2, where h_{FE1} and h_{FE3} are the common-emitter forward current transfer ratios of Q_1 and Q_3, respectively. Transistors Q_2 and Q_4 operate differentially with transistors Q_1 and Q_3, respectively.

Fig. 3 shows the test circuit diagram which corresponds to the basic circuit principle of a universal nullor Fig. 2 (d). The transistors Q_5, Q_6, Q_7, Q_9, Q_{10} and Q_{11} in Fig. 3 correspond to the constant current sources J_1, J_4, J_5, J_2, J_3 and J_6 in Fig. 2 (d), respectively.



Q_1, Q_2: 2SA798　　Q_3, Q_4 : 2SC1583
Q_5- Q_8: 2SA640　　Q_9- Q_{12}: 2SC1222
D_1- D_6: 1S1588　　V_S= ±15 [V]

Fig. 3. Test circuit diagram for Fig. 2 (d).



α : Current gain
i_b: Base Current
i_e: Emitter current
i_c: Collector current
r_b: Base resistance
r_e: Emitter resistance
r_c: Collector resistance

Fig. 4. T-equivalent circuit of a transistor, common-base configulation.

2.2 Analysis of The Practical Test Circuit for Fig. 2 (d)

The differential and common-mode input resistances, and the differential current gain of the circuit of Fig. 3 are calculated by using the T-equivalent circuit of a transistor shown

in Fig. 4 [7].

(1) Differential input resistance of the output stage :

$$R_{id2} = 2\left[r_{b2} + \frac{r_{e2}[\{r_{c3}//(R_L/2)\} + r_{c2}]}{\{r_{c3}//(R_L/2)\} + r_{c2}(1-\alpha_2) + r_{e2}}\right]^{*}.$$

(2) Common-mode input resistance of the output stage :

$$R_{ic2} = r_{b2} + \frac{(r_{e2}+2r_{c4})(r_{c3}+r_{c2})}{r_{c3}+r_{c2}(1-\alpha_2)+r_{e2}+2r_{c4}}.$$

(3) Differential input resistance (at the input stage) :

$$R_{id} = 2\left[r_{b1} + \frac{r_{e1}[\{r_{c4}//R_{ic2}//(R_{id2}/2)\} + r_{c1}]}{\{r_{c4}//R_{ic2}//(R_{id2}/2)\} + r_{c1}(1-\alpha_1) + r_{e1}}\right].$$

(4) Common-mode input resistance (at the input stage) :

$$R_{ic} = r_{b1} + \frac{(r_{e1}+2r_{c3})\{(r_{c4}//R_{ic2}) + r_{c1}\}}{(r_{c4}//R_{ic2}) + r_{c1}(1-\alpha_1) + r_{e1} + 2r_{c3}}.$$

(5) Differential current gain of the output stage :

$$A_{id2} = \frac{r_{c3}(\alpha_2 r_{c2} - r_{e2})}{\{r_{c3}+(R_L/2)\}\{r_{c2}(1-\alpha_2)+r_{e2}\} + r_{c3}(R_1/2)}.$$

(6) Differential current gain of the input stage :

$$A_{id1} = \frac{(r_{c4}//R_{ic2})(\alpha_1 r_{c1} - r_{e1})}{\{(r_{c4}//R_{ic2}) + (R_{id2}/2)\}\{r_{c1}(1-\alpha_1)+r_{e1}\} + (r_{c4}//R_{ic2})(R_{id2}/2)}.$$

(7) Differential current gain (in total) :

$$A_{id} = A_{id1}A_{id2}.$$

In the derivation of the above expressions, the internal resistances of the constant current sources Q_5 to Q_7 and Q_9 to Q_{11} are assumed to be equal to their collector resistances [8]. The notations used in the above expressions are as follows : (1) The subscripts of r_b, r_e, r_c and α, "1, 2, 3 and 4," correspond to the transistors 2SA798 (dual type), 2SC1583 (dual type), 2SA640 and 2SC1222, respectively. (2) R_L corresponds to the load resistor which may be connected between the output terminals 2 and 2′.

Substituting the following typical values of the transistors into the above expressions :

(1) Current gain: $\alpha \triangleq \alpha_1 = \alpha_2 = 0.995$,

(2) Base resistance : $r_b \triangleq r_{b1} = r_{b2} = 500\ [\Omega]$,

(3) Emitter resistance : $r_e \triangleq r_{e1} = r_{e2} = 25\ [\Omega]$,

(4) Collector resistance : $r_c \triangleq r_{c1} = r_{c2} = r_{c3} = r_{c4} = 5\times10^7\ [\Omega]$,

then the following values are obtained :

(1) $R_{id} = 10.8\ [k\Omega]$ for $r_c \gg (R_L/2)$, and $11.0\ [k\Omega]$ for $r_c \ll (R_L/2)$,

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* The notation "//" means the parallel connection; therefore, for example, $R_1//R_2 = R_1R_2/(R_1+R_2)$.

(2) $R_{ic} = 61.1$ [MΩ],

(3) $A_{id} = 92$ [dB].

Table 1. Experimental results of the universal nullor of Fig. 3

DC supply voltage: $V_S = \pm 15$ [V],	Temperature: $T_a = 20$ [°C]
(1) Differential voltage gain:	$A_{vd} = 100$ [dB] for $f \leqq 100$ [Hz] (98 [dB] at $f = 1$ [kHz])
(2) Common-mode voltage gain:	$A_{vC} = 40$ [dB] at $f = 1$ [kHz]
(3) Common-mode rejection ratio:	CMRR = 58 [dB] at $f = 1$ [kHz]
(4) Transition frequency:	$f_T = 35$ [MHz] at $R_L = \infty$ [Ω]
(5) Differential current gain:	$A_{id} = 92$ [dB] for $f \leqq 100$ [Hz]
(6) Differential input resistance:	$R_{id} = 12$ [kΩ] for $f \leqq 100$ [Hz]
(7) Common-mode input resistance:	$R_{iC} = 60$ [MΩ] for $f \leqq 1$ [kHz]
(8) Output resistance:	$R_o = 30$ [kΩ] for $f \leqq 100$ [Hz]
(9) Maximum output voltage:	$v_{omax} = \pm 13.5$ [V] for $R_L \geqq 5$ [kΩ]
(10) Maximum output current:	$i_{omax} = \pm 4.0$ [mA] for $R_L \leqq 5$ [kΩ]

2.3 Experimental Results

Table 1 shows the experimental results of the universal nullor of Fig. 3. The measured values of R_{id}, R_{iC} and A_{id} are approximately equal to the calculated values in the previous subsection. The practical test circuit of Fig. 3 has a lower differential input resistance R_{id} and a higher output resistance R_o in comparison with the usual operational amplifier, because the former is intrinsically a current controlled current source with large internal gain, while the latter is intrinsically a voltage controlled voltage source with large internal gain.

The frequency characteristics of the universal nullor of Fig. 3 are shown in Fig. 5.

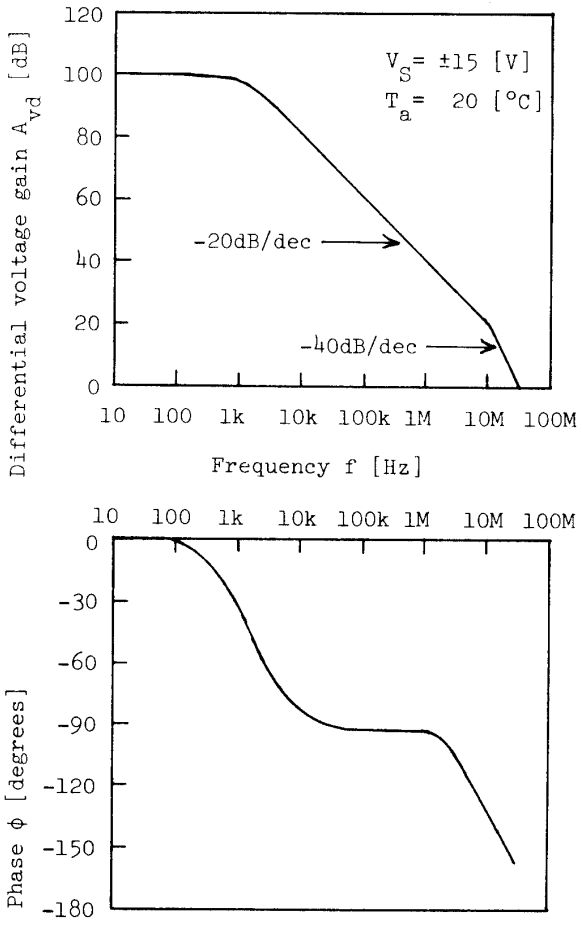


Fig. 5. Frequency characteristics of the universal nullor of Fig. 3.

3. Applications of Universal Nullors to The nct-α Type Two-Port Realization

The nct-α type two-port is defined as the noncommon-terminal type two-port having a cutset of nullators only and a cutset of norators only between port 1 and port 2 [1], [9], [10]. It satisfies the port condition that the current entering one terminal is equal to the current leaving the other terminal both in port 1 and in port 2, even if it is embedded in any network. Therefore, it can be used both in the common-terminal configulation and in the noncommon-terminal configulation, and can be used for an arbitrary network realization without any restrictions.

In the following subsections, the practical test circuit Fig. 3 of the universal nullor is applied to the realizations for the nct-α type voltage controlled current source and the current controlled voltage source, which are taken as the examples of the nct-α type two-port, and the insulation properties between ports 1 and 2 of the nct-α type two-ports are examined.

3.1 nct-α Type Voltage Controlled Current Source (VCCS)

Fig. 6 (a) shows the experimental circuit schematic of the nct-α type VCCS [4].

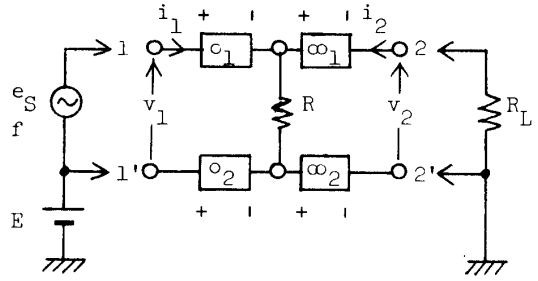
In Fig.'s 6 (a) and 7 (a), a nullator and a norator which are labeled by the same number compose a nullor, and the signs, + and −, of a nullor mean its polarities. Port 1 and port 2 must be electrically insulated each other because of the nct-α type.

The ideal characteristics of VCCS are $i_1 \equiv 0$ [A] and $i_2 = R^{-1} v_1$ [A].

Fig. 6 (b) shows the experimental results, where Experiment 1 is the case when the terminals 1′ and 2′ are grounded, Experiment 2 is the case when the terminal 1′ is provided the DC voltage E = 5 [V] and the terminal 2′ is grounded, Experiment 3 is the case when the terminals 1′ and 2 are grounded, and Experiment 4 is the case when the terminal 1′ is provided E = 5 [V] and the terminal 2 is grounded. The ideal value of mutual transfer conductance of VCCS is R^{-1} [S]. The experimental value of it is calculated by using the relation $g \triangleq -v_2/(v_1 R_L)$ [S], where v_1 and v_2 are the measured voltages of port 1 and port 2, respectively. Therefore, the relative error is expressed as $\varepsilon \triangleq (g - R^{-1})/R^{-1}$.

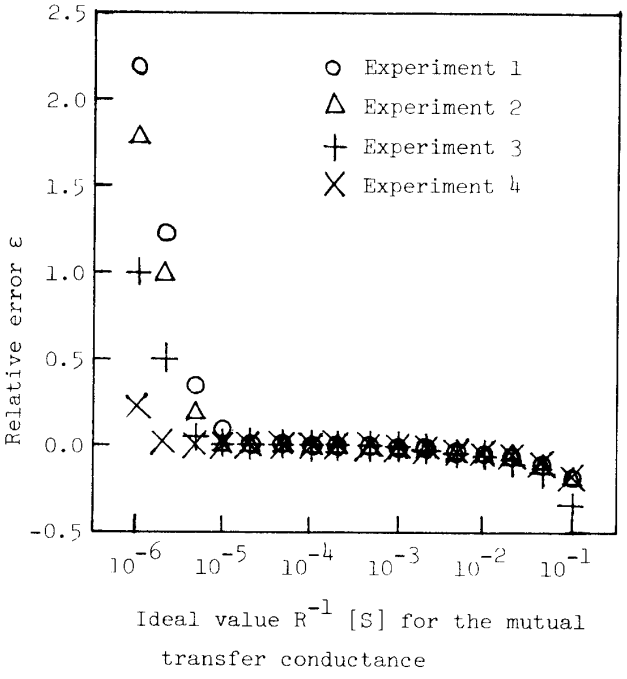
These experiments are performed for examining the electrical insulation property between ports 1 and 2 and the deviation of the practical circuit of nct-α type VCCS from the ideal model of it.

In Experiment 2, the DC level of terminal 2 is increased 0.4 [V] for $R^{-1} = 0$ to 10^{-1} [S] in comparison with Experiment 1. In Experiment 4, that of terminal 2′ is decreased 0.2 [V] for $R^{-1} = 0$ to 10^{-1} [S] in comparison with Experiment 3. These values concerning with the insulation property between ports 1 and 2 is the expectable values for practical use, because



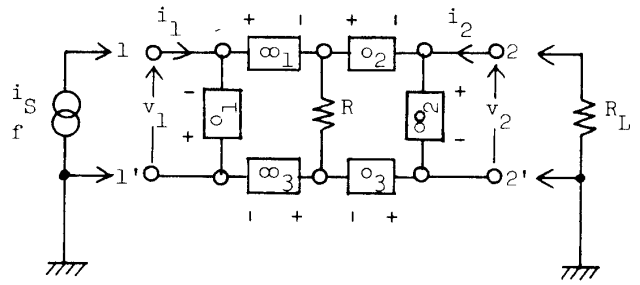
e_S: Independent voltage source, f= 1 [kHz]
R : Resistor for the mutual transfer conductance
R_L: Load resistor, R_L= 10 [kΩ]
E : DC voltage source, E= 0 [V], +5 [V]

(a) Experimental circuit schematic of the nct-α type VCCS.



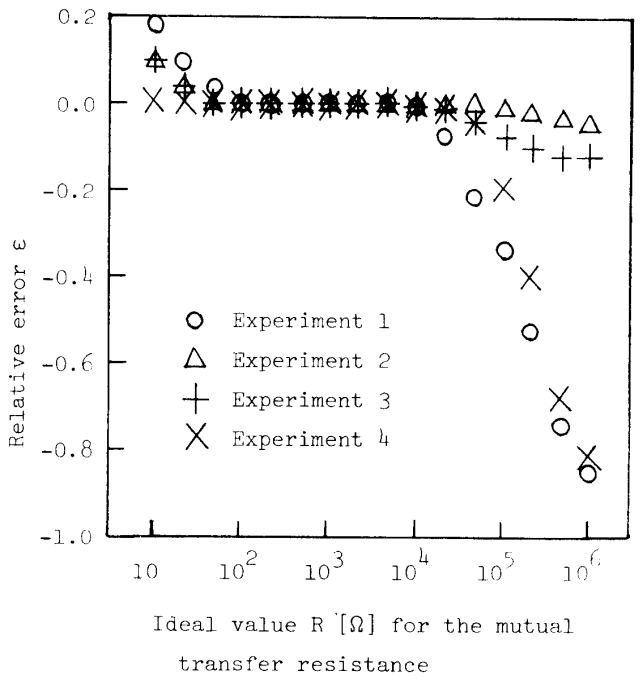
(b) Plot of the mutual transfer conductance.

Fig. 6. nct-α type VCCS.



i_S: Independent current source, f= 1 [kHz]
R : Resistor for the mutual transfer resistance
R_L: Load resistor, R_L= 10 [kΩ]

(a) Experimental circuit schematic of the nct-α type CCVS.



(b) Plot of the mutual transfer resistance.

Fig. 7. nct-α type CCVS.

this property is possible to be improved by selecting better active and passive elements for the implemented nullors and by more elabolate adjustments of the implemented nullors.

The linearity of mutual transfer conductance better than 1 percent is obtained in the range $R^{-1} = 2\times10^{-5}$ to 5×10^{-4} [S], and the linearity of it better than 10 percent is obtained in the range $R^{-1} = 10^{-5}$ to 2×10^{-2} [S] as shown in Fig.6(b). As R^{-1} is decreased in Experiments 1, 2, 3 and 4, the drift arises in port 2 as follows: (1) It is not observed at $R^{-1} \geqq 10^{-5}$ [S] in Experiments 1, 2, 3 and 4. (2) It is ±0.5 [V] with period T = 2 or 5 [min] at $R^{-1} = 10^{-6}$ [S] in Experiments 1 and 2. (3) It is ±0.1 [V] with period T= 1 or 2 [min] at $R^{-1} = 10^{-6}$ [S] in Experiments 3 and 4. When the frequency f is varied from 10 to 10^7 [Hz] at $R^{-1} = 10^{-3}$ [S]

in Experiment 1, $g = 10^{-3}$ [S] is measured.

In the case when the combination of nullator-norator pairs shown in Fig. 6 (a) is changed, the stability is worse than in the case of Fig. 6 (a). This can be checked by the algorithm [11] based on the return difference matrix.

3.2 nct-α Type Current Controlled Voltage Source (CCVS)

Fig. 7 (a) shows the experimental circuit schematic of the nct-α type CCVS. The ideal characteristics of CCVS is $v_1 \equiv 0$ [V] and $v_2 = Ri_1$[V].

Fig. 7 (b) shows the experimental results, where Experiment 1 is the case when the terminals 1′ and 2′ are grounded, Experiment 2 is the case when the terminals 1′ and 2 are grounded, Experiment 3 is the case when the terminals 1 and 2′ are grounded, and Experiment 4 is the case when the terminals 1 and 2 are grounded. The ideal value of mutual transfer resistance of CCVS is R [Ω]. The experimental value of it is calculated by using the relation $r \triangleq v_2/i_1$ [Ω], where i_1 and v_2 are the measured current of port 1 and the measured voltage of port 2, respectively. Therefore, the relative error is expressed as $\varepsilon \triangleq (r-R)/R$. In Experiments 2 and 4, the capacitor which is inserted between the collector and base of the negative output transistor of the implemented nullor labeled "2" in Fig. 7 (a), is taken 500 [pF], for the suppressing the about 10 [MHz] parasitic oscillation.

The insulation property between ports 1 and 2 and the deviation of the practical circuit of nct-α type CCVS from the ideal model of it are exmined.

When the DC voltage of E = 5 [V] is provided between the terminal 1 and the ground in Experiment 1, the following phenomena are obtained: (1) The DC level of the terminal 2 is varied -0.004, -0.04, -0.25, -1.8, -4.0 and -8.0 [V] at $R = 10$, 10^2, 10^3, 10^4, 10^5 and 10^6 [Ω], respectively. (2) For $R \leqq 2\times10^4$ [Ω], r is equal to the value measured when E = 0 [V], and for $R \geqq 5\times10^4$ [Ω], r is approximately equal to the value measured when E = 0 [V].

The linearity of mutual transfer resistance better than 1 percent is obtained in the range $R = 10^2$ to 10^4 [Ω], and the lineality of it better than 10 percent is obtained in the range $R = 2\times10$ to 2×10^4 [Ω] as shown in Fig. 7 (b).

As R is increased in Experiments 1, 2, 3 and 4, the drift arises in port 2. For example, it is not observed at $R \leqq 2\times10^4$ [Ω] in Experiments 1, 2, 3 and 4, but it is ±0.2, ±3.0, ±2.0 and ±1.0 [V] with period T = 1 or 2 [min] at $R = 10^6$ [Ω] in Experiments 1, 2, 3 and 4, respectively. When the frequency f is varied from 10 to 10^7 [Hz] at $R = 10^3$ [Ω] in Experiment 1, $r = 10^3$ [Ω] at $f \leqq 2\times10^6$ [Hz], $r = 0.95\times10^3$ [Ω] at $f = 5\times10^6$ [Hz], and $r = 0.9\times10^3$ [Ω] at $f = 10^7$ [Hz] are measured.

The combination of nullator-norator pairs shown in Fig. 7 (a) is superior in the stability

to another combination. The reason for this is as follows: The circuit of Fig. 7 (a) is constructed only by the three-terminal nullors, but when another combination of nullator-norator pairs is selected, at least one four-terminal nullor is needed ; therefore, in the latter case, the negative feedback of the practical circuits of nullor is not sufficiently provided.

4. Conclusion

The implementation of the balanced and universal nullor has been examined in the simple practical circuit shown in Fig. 3 which is based on the circuit principle diagram of Fig. 2 (d). The implemented circuit of it has been applied to the nct-α type VCCS and CCVS realizations. The electrical insulation property between port 1 and port 2 was examined in datail. This property has been shown to be expectable for practical use, in consideration of the possibility of improving the property by more elabolate design and adjustment of the implementation of nullor. The operations of VCCS and CCVS have been staisfactory. The availability of nct-α type two-port has been confirmed.

The implementation of the universal nullor having the fully floating input and output ports is very usefull to the designer of accurate analog electronic systems in minimizing the required number of active elements and passive precision elements.

References

[1] T. Matsumoto and Y. Kato, "Unified synthesis of all active and nonreciprocal network elements using nullator-norator pairs," Paper of Technical Group, TGCST74-21, IECE of Japan, May 1974 (in Japanese).

[2] J. H. Huijsing and J. de Korte, "Monolithic nullor—A universal active network element," IEEE J. Solid-State Circuits, vol. SC-12, no. 1, pp. 59-64, Feb. 1977.

[3] H. J. Carlin, "Singular network elements," IEEE Trans. Circuit Theory, vol. CT-11, no. 1, pp. 67-72, Mar. 1964.

[4] Y. Kato and T. Matsumoto,"An implementation of ungrounded four-terminal nullor," Convention Records of Hokuriku Section of I. E. E. I. T. of Japan, B-24, Oct. 1977 (in Japanese).

[5] W. H. Cornetet and F. E. Battocletti, Electronic circuits by system and computer analysis. Chap. 5, Tokyo: McGraw-Hill Kogakusha, 1975.

[6] The op amp manual. Tokyo: CQ-Shuppan, 1978 (in Japanese).

[7] M. Kawakami, Transistor and its circuits 1. Chap.'s 1 and 2, Tokyo: Kyoritsu-Shuppan, 1974 (in Japanese).

[8] J. G. Graeme and G. E. Tobey, Operational amplifiers, Design and applications. Tokyo: McGraw-Hill Kogakusha, 1971.

[9] T. Matsumoto and Y. Kato, "Equivalent controlled source networks with nullators and norators," Trans. IECE of Japan, vol. 57-A, no. 8, pp. 630-632, Aug. 1974 (in Japanese).

[10] T. Matsumoto, "Minimal realizations of controlled sources using nullors and positive resistors," Trans. IECE of Japan, vol. J59-A, no. 5, pp. 423-425, May 1976 (in Japanese).

[11] Y. Kato and T. Matsumoto, "An algorithm of replacing nullors of the nullor-modeled resistive network with operational amplifiers," Convention Records of Hokuriku Section of I. E. E. I. T. of Japan, B-15, Oct.1978 (in Japanese).